### -60V P+P-Channel Enhancement Mode MOSFET

#### **Description**

The AP6V06S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = -60V I_{D} = -6A$ 

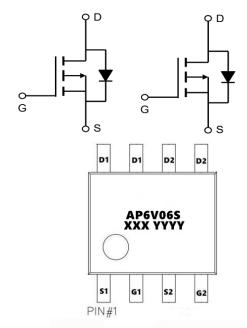
 $R_{DS(ON)} < 85m\Omega$  @  $V_{GS}=10V$  (Type:  $65m\Omega$ )

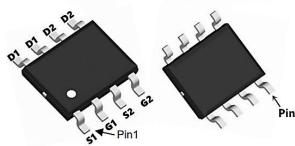
#### **Application**

Brushless motor

Load switch

Uninterruptible power supply





**Package Marking and Ordering Information** 

Product ID	Pack	Marking	Qty(PCS)		
AP6V06S	SOP-8L	AP6V06S XXX YYYY	3000		

Absolute Maximum Ratings (T<sub>c</sub>=25°Cunless otherwise noted)

Symbol	Parameter Rating		Units	
V <sub>D</sub> s	Drain-Source Voltage	-60	V	
V <sub>G</sub> s	Gate-Source Voltage	Gate-Source Voltage ±20		
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup> -6		
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup> -4.3		А	
Ірм	Pulsed Drain Current <sup>2</sup>	Pulsed Drain Current <sup>2</sup> -26		
EAS	Single Pulse Avalanche Energy <sup>3</sup> 29.8		mJ	
las	Avalanche Current	-24.4		
$P_D@T_C=25^{\circ}C$	Total Power Dissipation⁴	31.3	W	
Тѕтс	Storage Temperature Range	-55 to 150	°C	
TJ	Operating Junction Temperature Range -55 to 150		°C	
Reja	Thermal Resistance Junction-Ambient <sup>1</sup>	85	°C/W	
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	40	°C/W	



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### P-Channel Electrical Characteristics (TJ =25 $^{\circ}$ C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-60	-66		V	
∆BVDSS/∆TJ	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA		-0.03		V/°C	
DDG(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-3A		65	85	mΩ	
RDS(ON)		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-2A		80	100	11122	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_{D}$ =-250uA	-1.2	1.75	-2.5	V	
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-48V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA	
וטסס		V <sub>DS</sub> =-48V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5		
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA	
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-3A		8.5		S	
Qg	Total Gate Charge (-4.5V)			12.1			
Qgs	Gate-Source Charge	$V_{DS}$ =-48V , $V_{GS}$ =-4.5V , $I_{D}$ =-3A		2.2		nC	
Qgd	Gate-Drain Charge			6.3			
Td(on)	Turn-On Delay Time			9.2			
Tr	Rise Time	V <sub>DD</sub> =-15V , V <sub>GS</sub> =-10V ,		20.1			
Td(off)	Turn-Off Delay Time	$R_G=3.3$ , $I_D=-1A$		46.7		ns	
Tf	Fall Time			9.4			
Ciss	Input Capacitance			1137			
Coss	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		76		pF	
Crss	Reverse Transfer Capacitance			50			
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-13	Α	
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C			-1.2	٧	

#### Note:

- 1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2. The data tested by pulsed , pulse width  $\, \leqq \, 300 us$  , duty cycle  $\, \leqq \, 2\%$
- 4. The data is theoretically the same as I D and I DM, in real applications, should be limited by total power dissipation.



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#### **P-Channel Typical Characteristics**

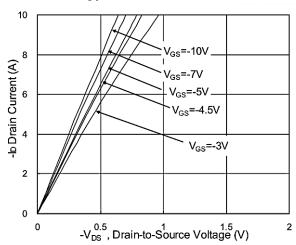


Fig.1 Typical Output Characteristics

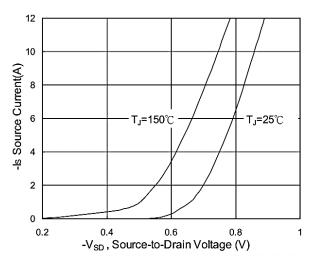


Fig.3 Forward Characteristics of Reverse

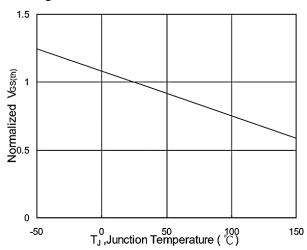


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$ 

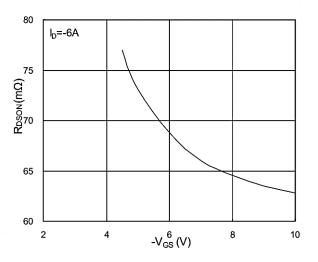


Fig.2 On-Resistance v.s Gate-Source

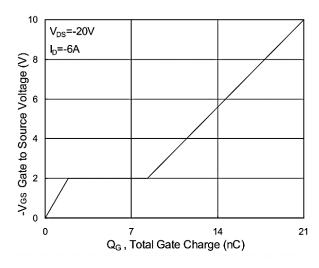


Fig.4 Gate-Charge Characteristics

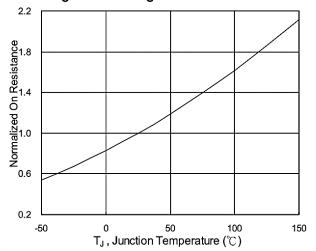
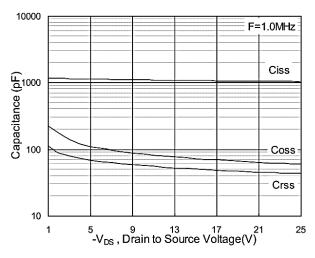


Fig.6 Normalized  $R_{DSON}$  v.s  $T_J$ 

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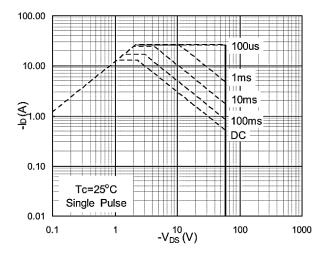
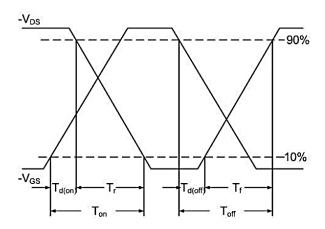


Fig.8 Safe Operating Area Fig.7 Capacitance Normalized Thermal Response (Reac) DUTY=0.5 0.1 0.05 0.02 SINGLE  $D = T_{ON}/T$  $T_J peak = T_C + P_{DM} \times R_{\theta JC}$ 0.001 0.00001 0.0001 0.001 0.01 0.1 10 t, Pulse Width (s)

Fig.9 Normalized Maximum Transient Thermal Impedance





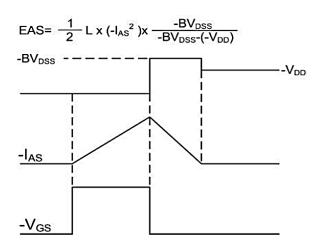
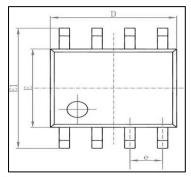


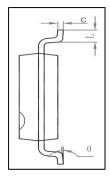
Fig.11 Unclamped Inductive Switching Waveform

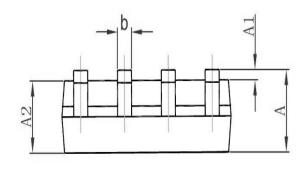


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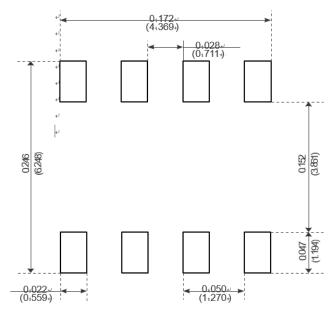
# Package Mechanical Data-SOP-8L







Symbol	Dimensions Ir	n Millimeters	Dimensions	In Inches
	Min	Max	Min	Max
Α	1. 350	1. 750	0. 053	0.069
A1	0. 100	0. 250	0. 004	0. 010
A2	1. 350	1. 550	0. 053	0. 061
b	0. 330	0. 510	0. 013	0. 020
С	0. 170	0. 250	0.006	0. 010
D	4. 700	5. 100	0. 185	0. 200
E	3. 800	4. 000	0. 150	0. 157
E1	5. 800	6. 200	0. 228	0. 244
е	1. 270 (BSC)		0. 050 (BSC)	
L	0. 400	1. 270	0. 016	0. 050
θ	0°	8°	0°	8°



Recommended Minimum Pads-