# AP30H04NF

## 40V N+N-Channel Enhancement Mode MOSFET

### Description

The AP30H04NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS}$ = 40V $I_D$ =30A

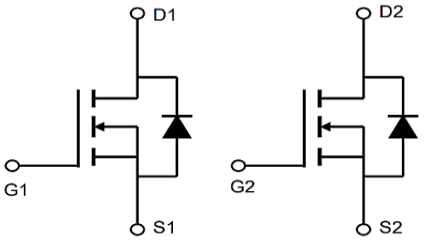
$R_{DS(ON)}$ < 14mΩ @ $V_{GS}$=10V （**Type：11mΩ**）

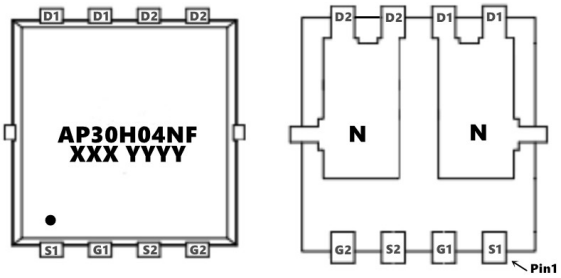
### Application

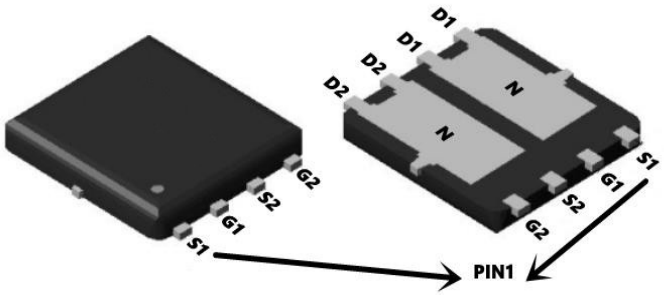
Wireless charging

Boost driver

Brushless motor




### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP30H04NF | PDFN5*6-8L | AP30H04NF XXX YYYY | 5000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDS | Drain-Source Voltage | 40 | V |
| VGS | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_A$=25℃ | Continuous Drain Current[1] | 30 | A |
| $I_D$@$T_A$=70℃ | Continuous Drain Current[1] | 21 | A |
| IDM | Pulsed Drain Current[2] | 36 | A |
| EAS | Single Pulse Avalanche Energy[3] | 31 | mJ |
| IAS | Avalanche Current | 25 | A |
| $P_D$@$T_A$=25℃ | Total Power Dissipation[4] | 1.9 | W |
| TSTG | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| $R_{\theta JA}$ | Thermal Resistance Junction-ambient[1](t≤10s) | 25 | ℃/W |
| $R_{\theta JC}$ | Thermal Resistance Junction-ambient[1] | 8 | ℃/W |

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### Electrical Characteristics ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| BVDSS | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 40 | 44 | --- | V |
| △BVDSS/△TJ | BVDSS Temperature Coefficient | Reference to 25℃ , $I_D$=1mA | --- | 0.034 | --- | V/℃ |
| RDS(ON) | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V , $I_D$=8A | --- | 11 | 14 | mΩ |
| | | $V_{GS}$=4.5V , $I_D$=6A | --- | 13 | 18 | |
| VGS(th) | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 1.0 | 1.6 | 2.5 | V |
| △$V_{GS(th)}$ | $V_{GS(th)}$ Temperature Coefficient | | --- | -5.64 | --- | mV/℃ |
| IDSS | Drain-Source Leakage Current | $V_{DS}$=32V , $V_{GS}$=0V , $T_J$=25℃ | --- | --- | 1 | uA |
| | | $V_{DS}$=32V , $V_{GS}$=0V , $T_J$=55℃ | --- | --- | 5 | |
| IGSS | Gate-Source Leakage Current | $V_{GS}$=±20V , $V_{DS}$=0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=8A | --- | 36 | --- | S |
| $R_g$ | Gate Resistance | $V_{DS}$=0V , $V_{GS}$=0V , f=1MHz | --- | 2.1 | --- | Ω |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=20V , $V_{GS}$=4.5V , $I_D$=8A | --- | 10.7 | --- | nC |
| Qgs | Gate-Source Charge | | --- | 3.3 | --- | nC |
| Qgd | Gate-Drain Charge | | --- | 4.2 | --- | nC |
| Td(on) | Turn-On Delay Time | $V_{DD}$=12V $V_{GS}$=10V $R_G$=3.3Ω $I_D$=6A | --- | 8.6 | --- | ns |
| $T_r$ | Rise Time | | --- | 3.4 | --- | ns |
| Td(off) | Turn-Off Delay Time | | --- | 24.8 | --- | ns |
| $T_f$ | Fall Time | | --- | 2.2 | --- | ns |
| Ciss | Input Capacitance | $V_{DS}$=15V , $V_{GS}$=0V , f=1MHz | --- | 1314 | --- | pF |
| Coss | Output Capacitance | | --- | 120 | --- | |
| Crss | Reverse Transfer Capacitance | | --- | 88 | --- | |
| IS | Continuous Source Current[1,5] | $V_G$=$V_D$=0V , Force Current | --- | --- | 8.5 | A |
| ISM | Pulsed Source Current[2,5] | | --- | --- | 34 | A |
| VSD | Diode Forward Voltage[2] | $V_{GS}$=0V , $I_S$=1A , $T_J$=25℃ | --- | --- | 1.2 | V |

**Note :**

1、The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、EAS condition: TJ=25℃, VDD=32V,VGS=10V,L=0.1Mh,IAS=22A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

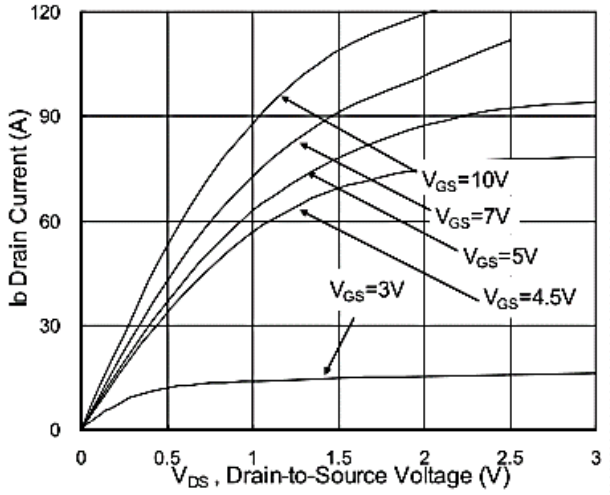


Fig.1 Typical Output Characteristics

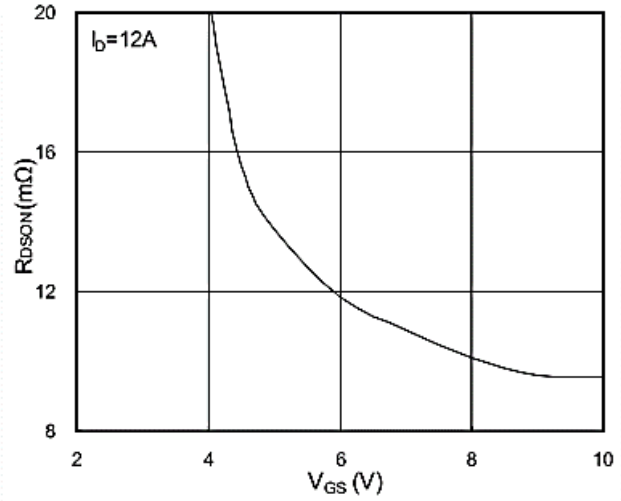


Fig.2 On-Resistance vs. G-S Voltage

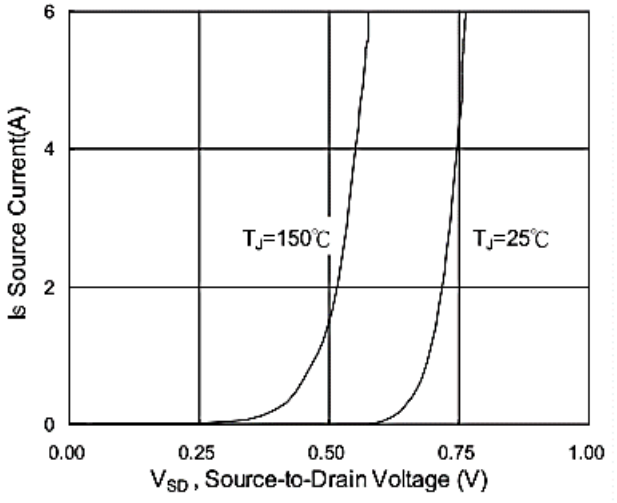


Fig.3 Forward Characteristics of Reverse

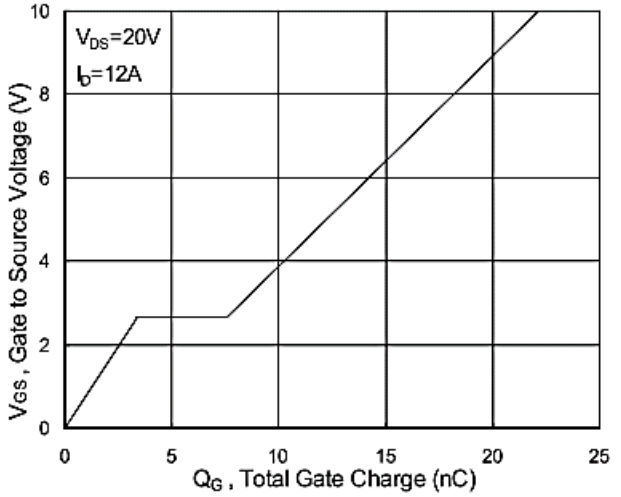


Fig.4 Gate-Charge Characteristics

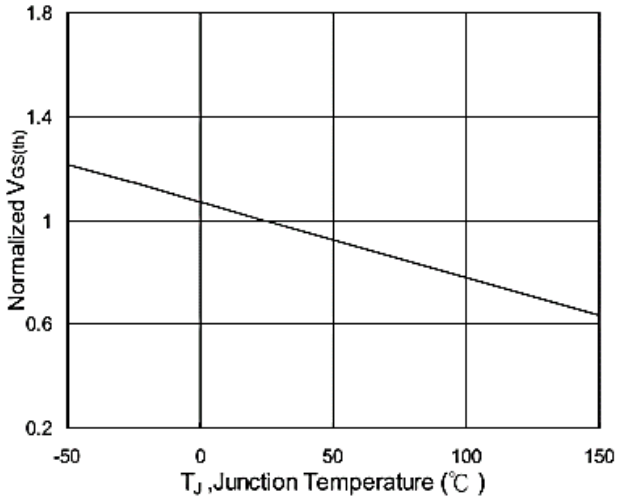


Fig.5 $V_{GS(th)}$ vs. $T_J$

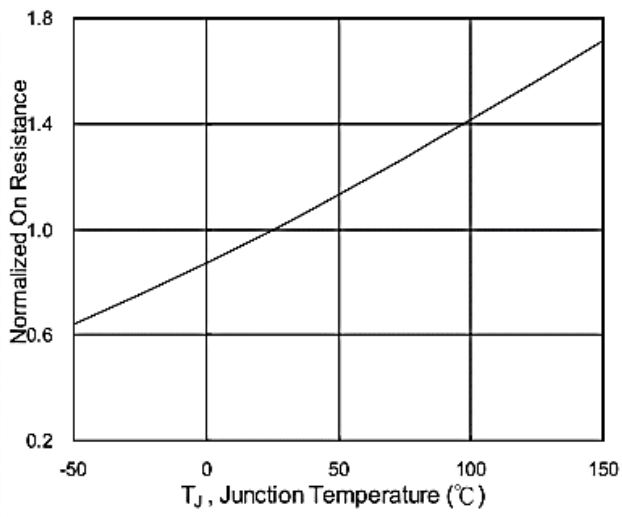


Fig.6 Normalized $R_{DSON}$ vs. $T_J$

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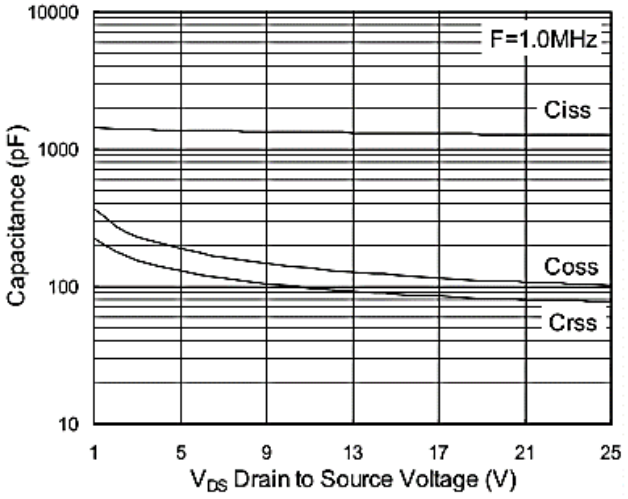



Fig.7 Capacitance

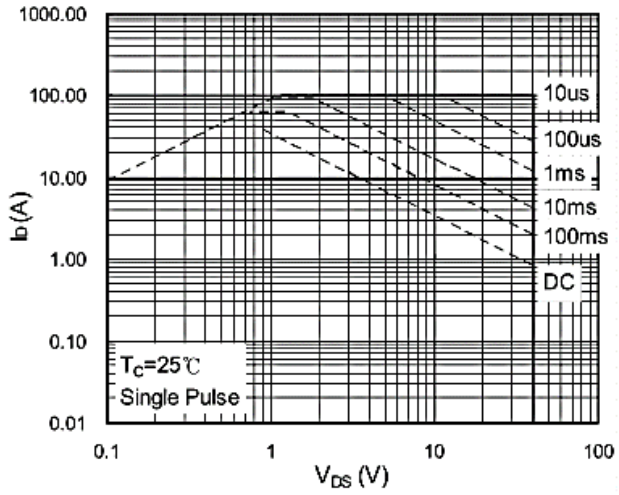



Fig.8 Safe Operating Area

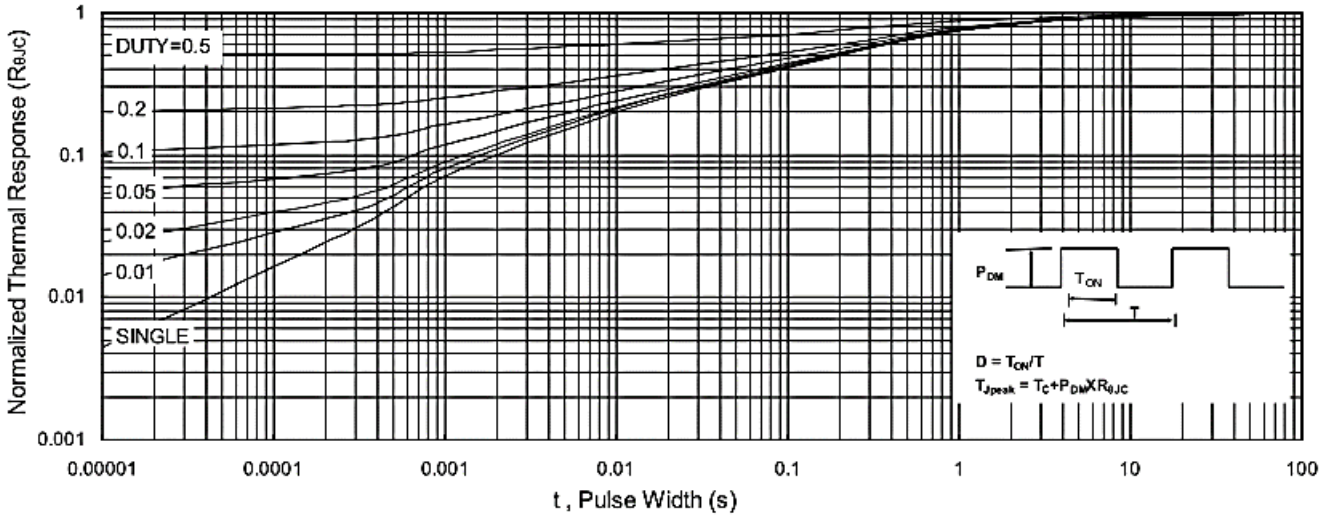



Fig.9 Normalized Maximum Transient Thermal Impedance

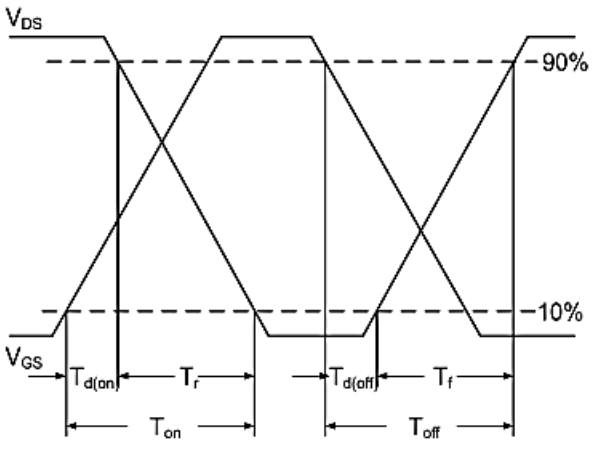



Fig.10 Switching Time Waveform

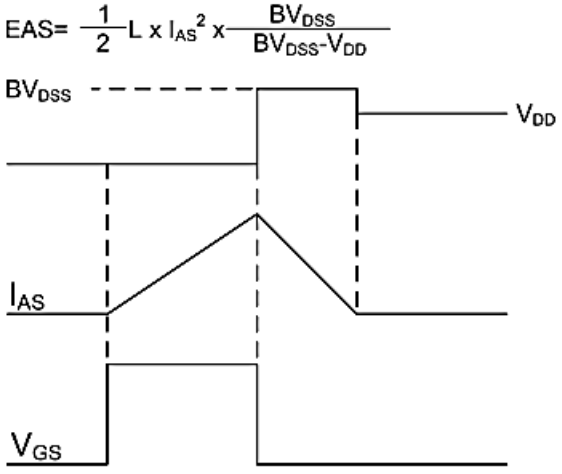
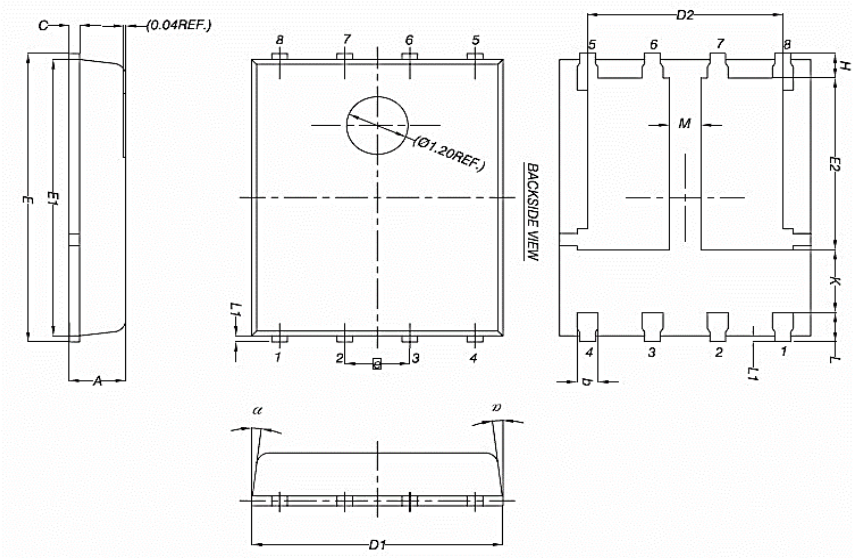



Fig.11 Unclamped Inductive Switching Waveform

## Package Mechanical Data-DFN5*6-8L-JQ Double




| Symbol | Common | | |
|---|---|---|---|
| | mm | | |
| | Mim | Nom | Max |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| C | 0.20 | 0.25 | 0.30 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 3.96 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 3.30 | 3.45 |
| E2 | 3.38 | 3.05 | 3.20 |
| e | 1.27BSC | | |
| H | 0.41 | 0.51 | 0.61 |
| K | 1.10 | -- | -- |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| M | 0.50 | -- | -- |
| a | 0° | -- | 12° |