

## 40V N+N-Channel Enhancement Mode MOSFET

### Description

The AP15H04S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 15A$

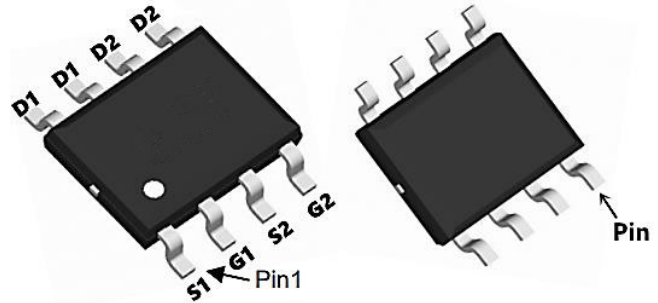
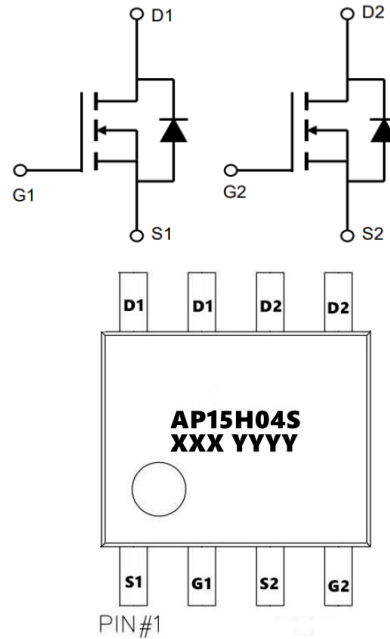
$R_{DS(ON)} < 10m\Omega$  @  $V_{GS}=10V$  (Type: **8.5m $\Omega$** )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15H04S	SOP-8L	AP15H04S XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	15	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	45	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	181	mJ
$I_{AS}$	Avalanche Current	16	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	33.7	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.1	$^\circ\text{C/W}$



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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

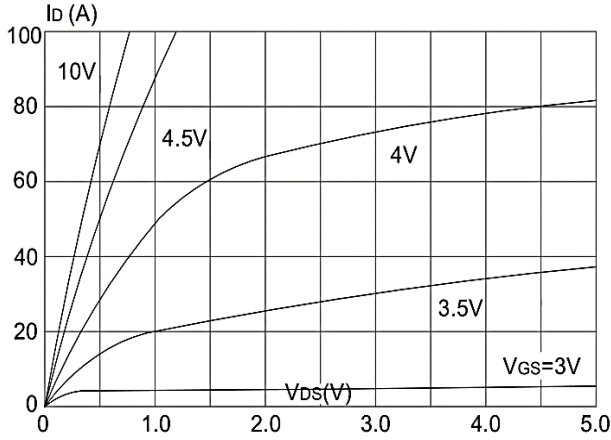
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	40	---	---	V
ΔBVDSS/ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.028	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	---	8.5	10	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	---	10	16	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.6	2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-6.16	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =30A	---	22	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.7	3.4	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V, V <sub>GS</sub> =10V, I <sub>D</sub> =25A	---	37	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	6	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	7	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, R <sub>G</sub> =1Ω I <sub>D</sub> =25A	---	12	---	ns
T <sub>r</sub>	Rise Time		---	12	---	
Td(off)	Turn-Off Delay Time		---	38	---	
T <sub>f</sub>	Fall Time		---	9	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz	---	2400	---	pF
C <sub>oss</sub>	Output Capacitance		---	192	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	165	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	50	A
ISM	Pulsed Source Current <sup>2,5</sup>		---	---	200	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>s</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	IF=30A, dI/dt=100A/μs, T <sub>J</sub> =25°C	---	22	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	11	---	nC

#### Note :

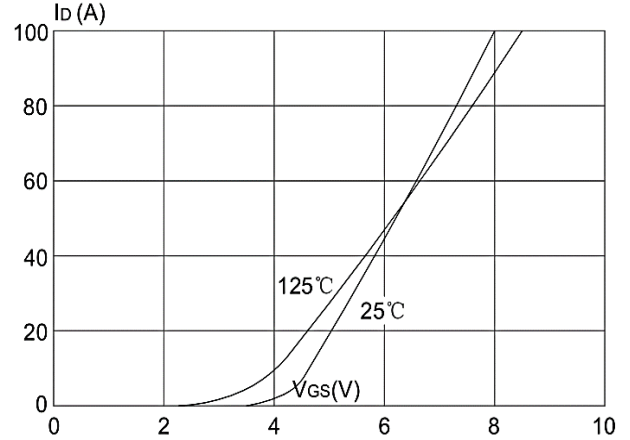
- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation

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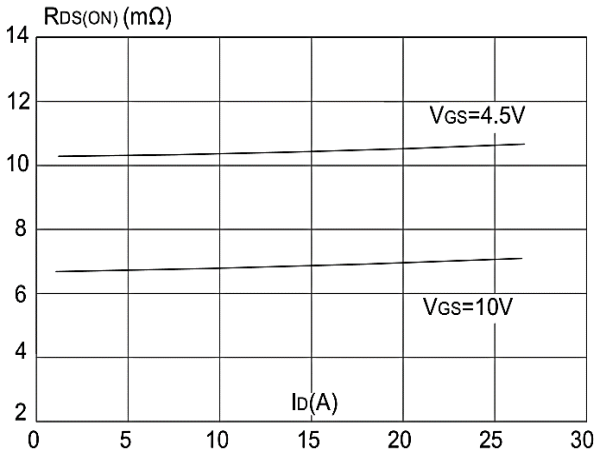
**Typical Characteristics**



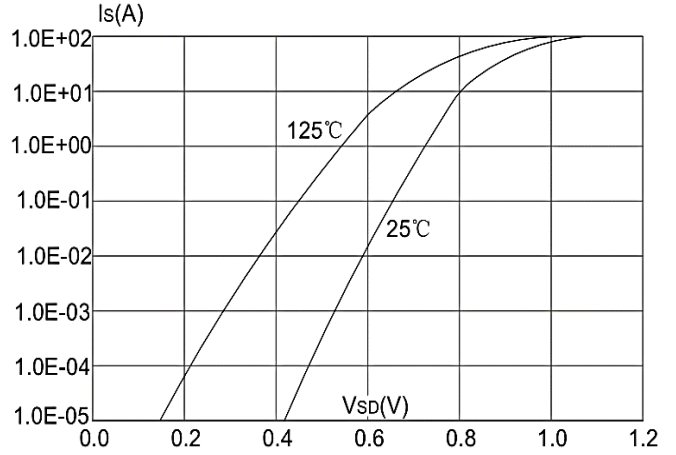
**Figure 1: Output Characteristics**



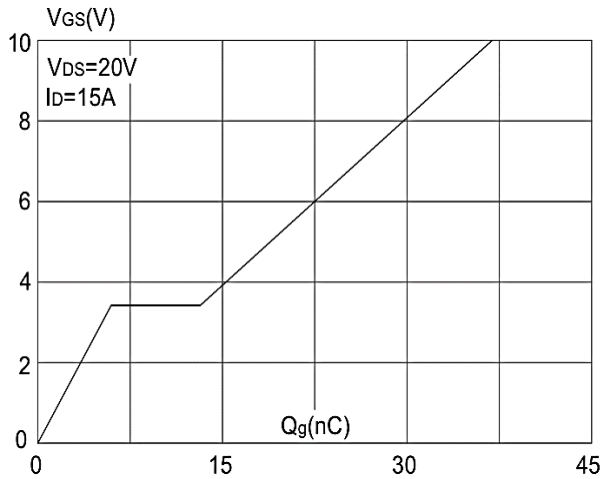
**Figure 2: Typical Transfer Characteristics**



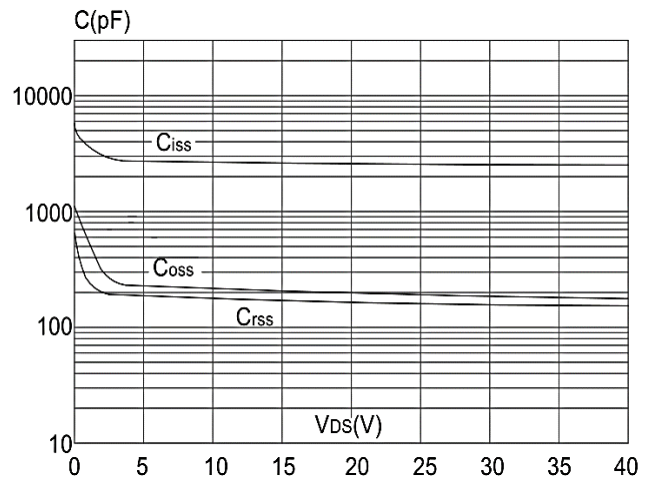
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**

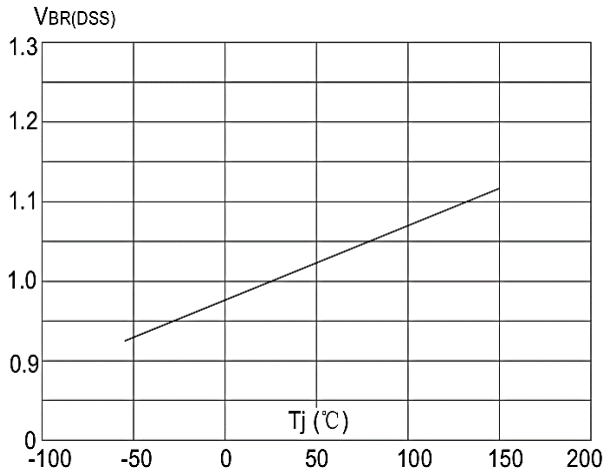


**Figure 5: Gate Charge Characteristics**

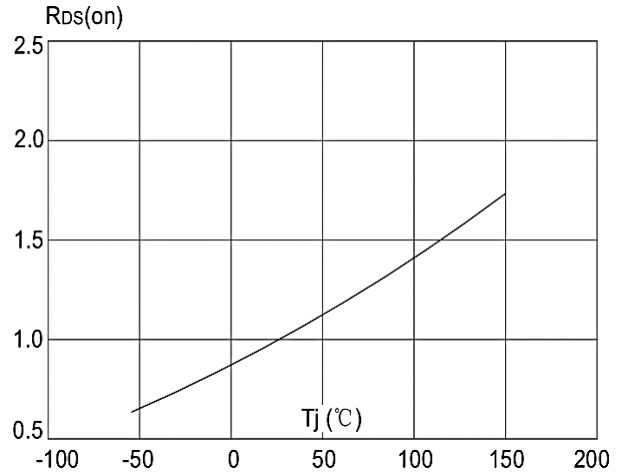


**Figure 6: Capacitance Characteristics**

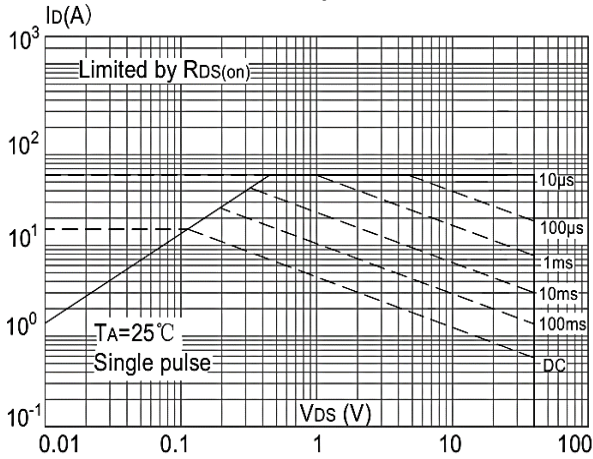
**40V N+N-Channel Enhancement Mode MOSFET**



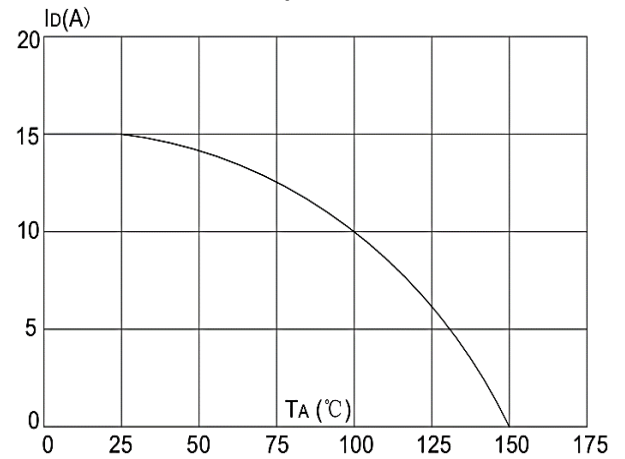
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



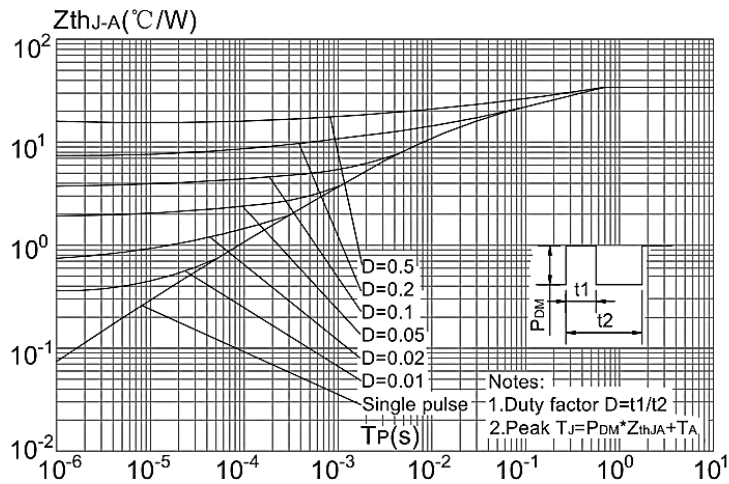
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area vs. Case Temperature**

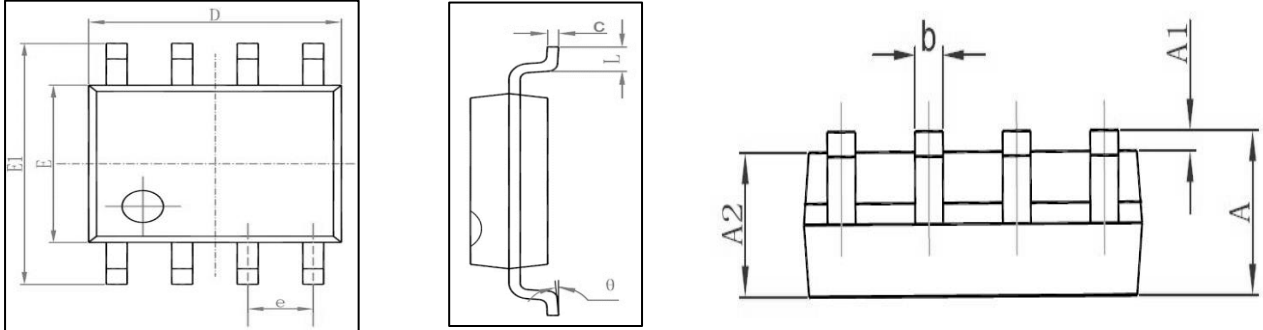


**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**

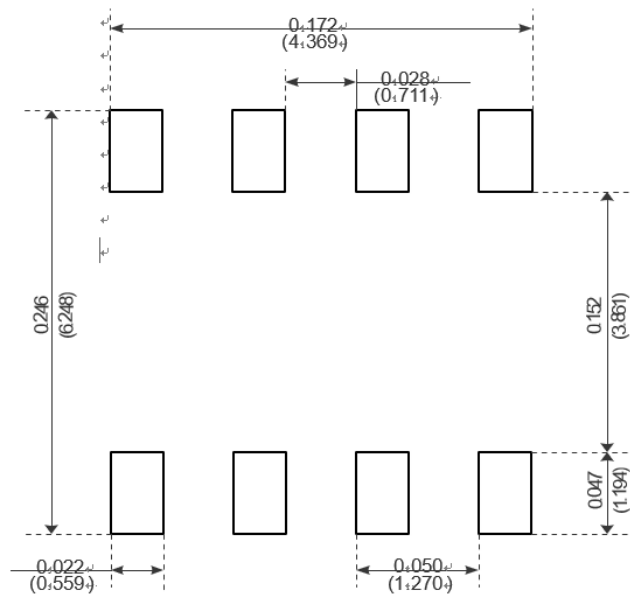


**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case**

### Package Mechanical Data-SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads