

12V N+N-Channel Enhancement Mode MOSFET

General Description

The AP8804DF is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the small power switching and load switch applications. They meet the RoHS and Product requirement with full function reliability approved.

General Features

$V_{DS} = 12V$ $I_D = 40A$

$R_{DS(ON)} < 4.3m\Omega$ @ $V_{GS}=4.5V$

$R_{DS(ON)} < 5.6m\Omega$ @ $V_{GS}=2.5V$

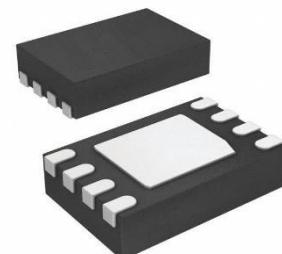
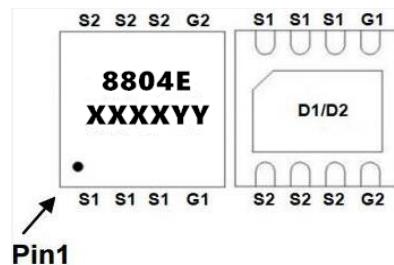
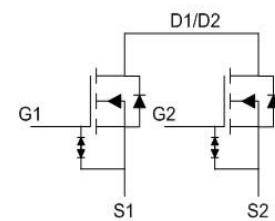
ESD=2KV HBM

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8804DF	WQDFN3*3-8L	8804E	5000

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	12	V
V_{GS}	Gate-Source Voltage	± 8	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V ¹	40	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V ¹	35.6	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V ¹	19	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V ¹	15	A
I_{DM}	Pulsed Drain Current ²	100	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ¹	31	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ¹	3.6	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	35	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	4	°C/W

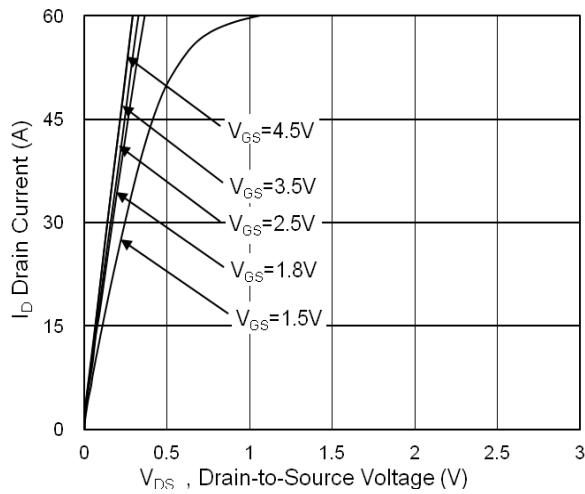
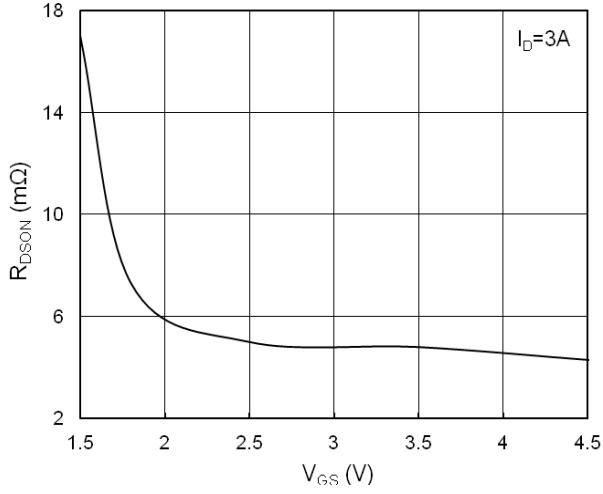
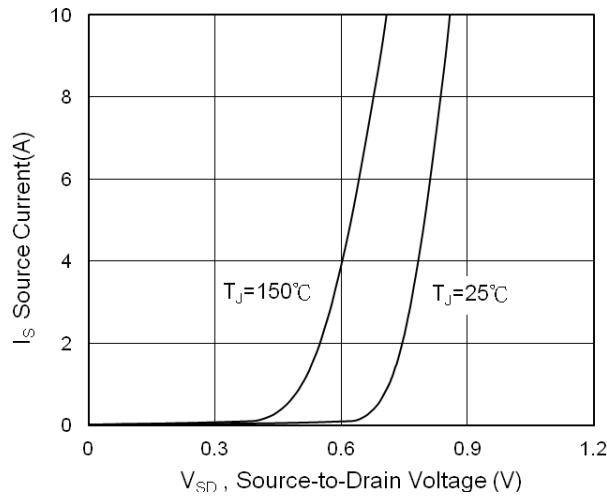
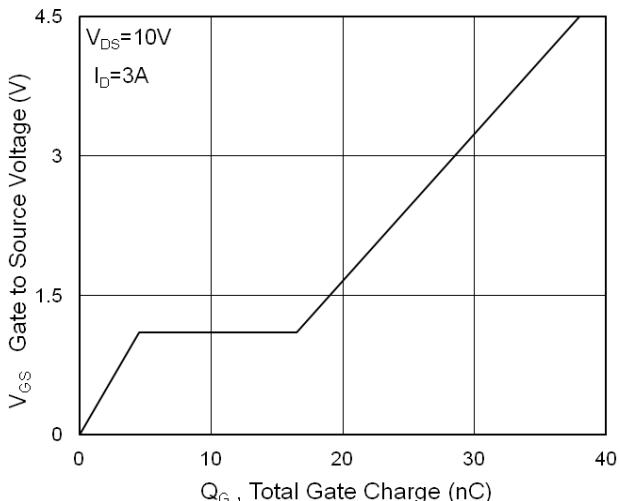
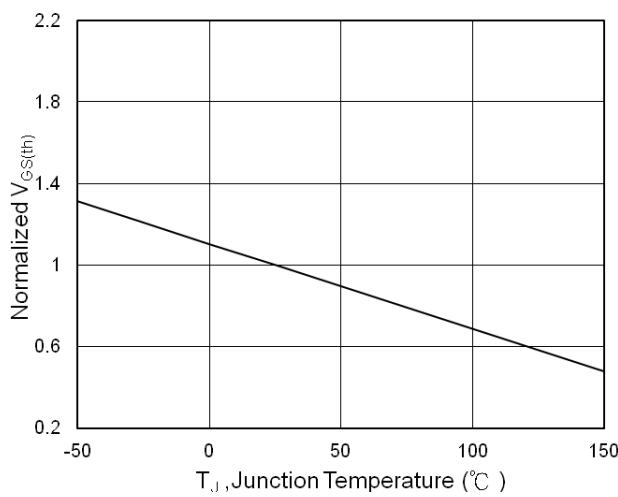
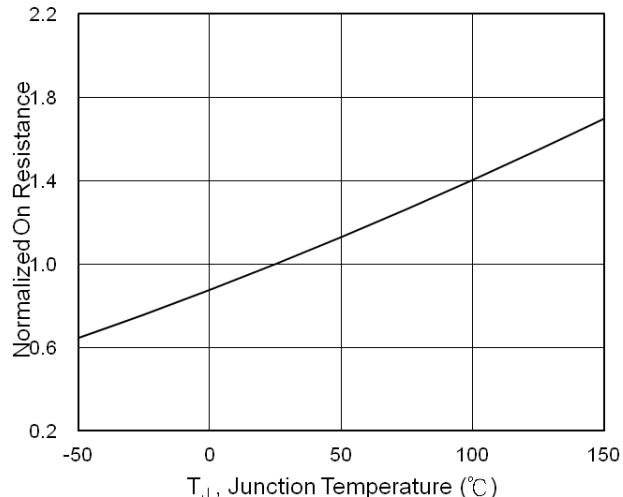
20V N+N-Channel Enhancement Mode MOSFET
N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

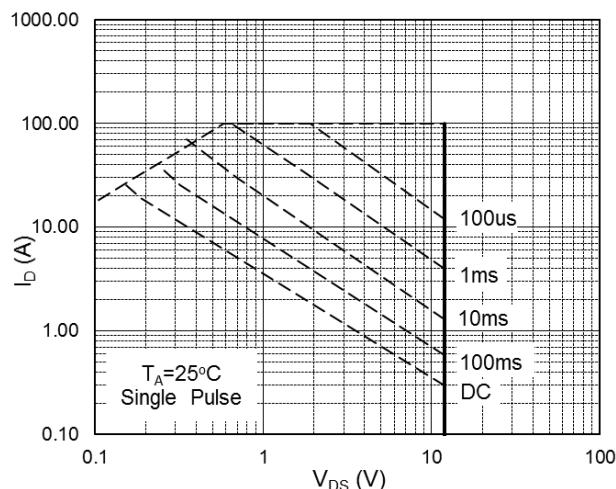
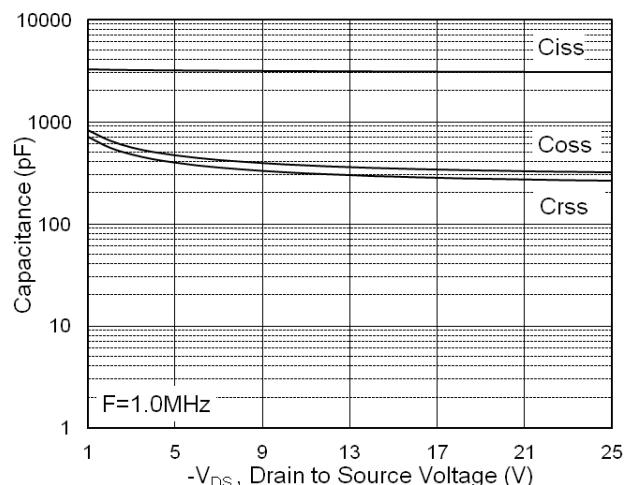
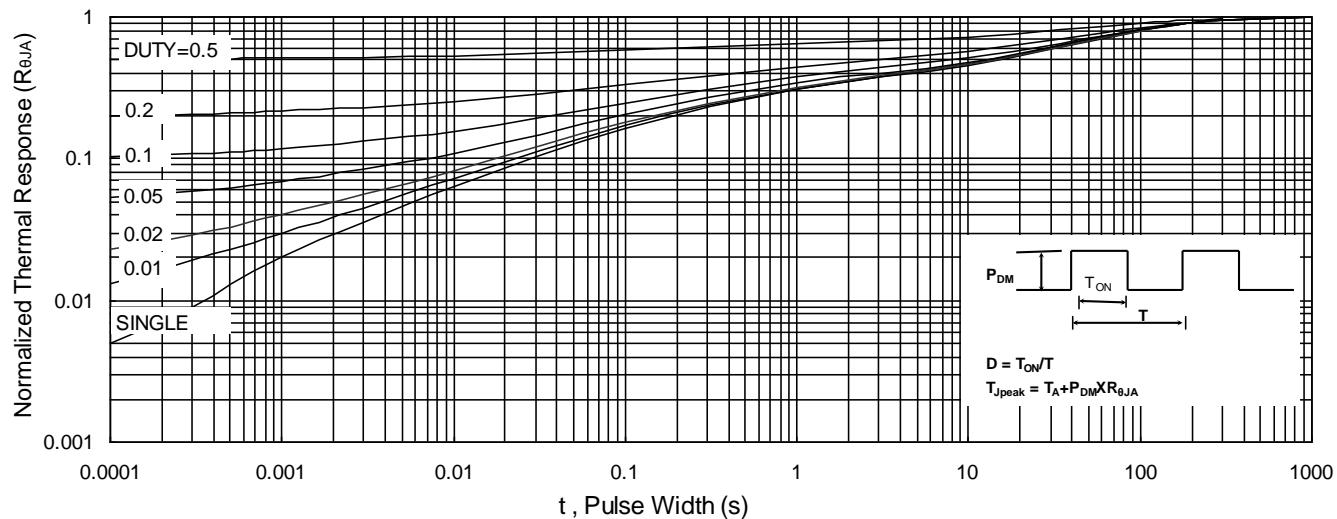
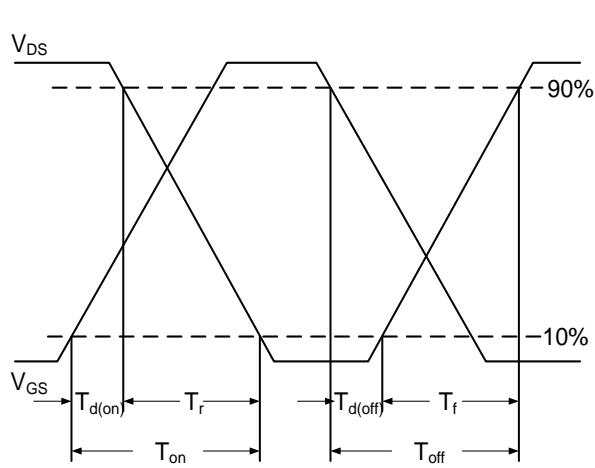
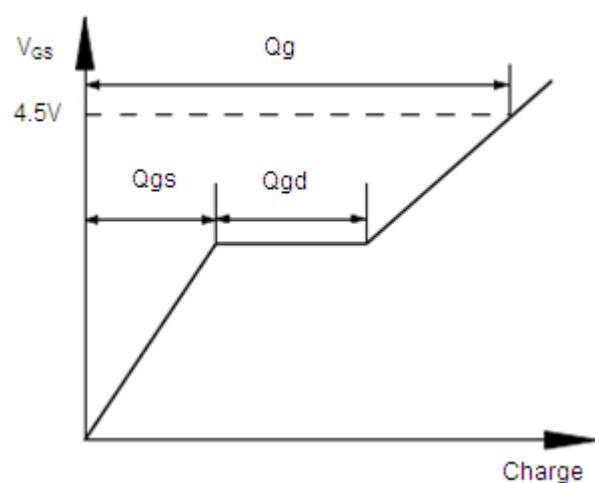
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	12	18	21	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=4.5\text{V}$, $I_D=3\text{A}$	2.3	3.3	4.3	$\text{m}\Omega$
		$V_{\text{GS}}=4.0\text{V}$, $I_D=3\text{A}$	2.4	3.4	4.4	
		$V_{\text{GS}}=3.1\text{V}$, $I_D=3\text{A}$	2.6	3.6	4.7	
		$V_{\text{GS}}=2.5\text{V}$, $I_D=3\text{A}$	3	4	5.6	
		$V_{\text{GS}}=1.8\text{V}$, $I_D=3\text{A}$	4	5.4	7.6	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	0.4	0.6	1.0	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=12\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=12\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 8\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 10	uA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=3\text{A}$	---	42	---	S
Q_g	Total Gate Charge (4.5V)	$V_{\text{DS}}=10\text{V}$, $I_D=3\text{A}$	---	38	---	nC
	Total Gate Charge (3.9V)		---	33	---	
Q_{gs}	Gate-Source Charge		---	4.5	---	
Q_{gd}	Gate-Drain Charge		---	12	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=10\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $R_G=6\Omega$ $I_D=3\text{A}$	---	22	---	ns
T_r	Rise Time		---	41	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	77	---	
T_f	Fall Time		---	21	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=10\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	3165	---	pF
C_{oss}	Output Capacitance		---	380	---	
C_{rss}	Reverse Transfer Capacitance		---	325	---	
I_s	Continuous Source Current ¹	$V_G=V_D=0\text{V}$, Force Current	---	---	30	A
I_{SM}	Pulsed Source Current ²		---	---	100	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=3\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

1 . The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $t \leq 10\text{s}$.

2.The data tested by pulsed , pulse width $\leq 10\text{us}$, duty cycle $\leq 1\%$

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Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. Gate-Source Voltage

Fig.3 Source Drain Forward Characteristics

Fig.4 Gate-Charge Characteristics

Fig.5 $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J


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Fig.7 Safe Operating Area

Fig.8 Capacitance

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform

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DFN3*3-XW-01

