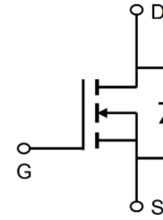
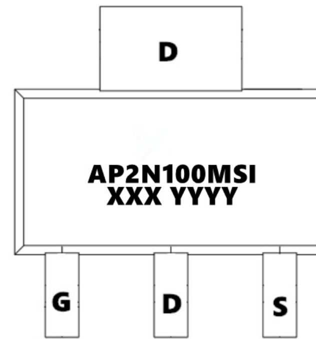
AP2N100MSI

1000V N-Channel Enhancement Mode MOSFET

Description

The AP2N100MSI is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





General Features

V_{DS} = 1000V I_D =1.7A

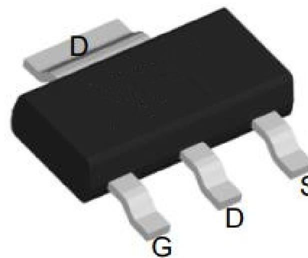
$R_{DS(ON)}$ < 9600mΩ @ V_{GS}=10V （Type：8000mΩ）

Application

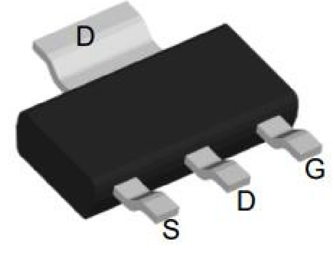
Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)

Top View



Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2N100MSI	SOT223-3L	AP2N100MSI XXX YYYY	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Units
VDSS	Drain-Source Voltage	1000	V
VGS	Gate-Source Voltage	±30	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	1.7	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	0.8	A
IDM	Drain Current - Pulsed	6	A
EAS	Single Pulsed Avalanche Energy	90	mJ
IAR	Avalanche Current	3	A
EAR	Repetitive Avalanche Energy	0.36	mJ
P_D	Power Dissipation	36	W
Tj ,Tstg	Operating and Storage Temperature Range	-55 to +150	oC
RθJC	Thermal Resistance, Junction-to-Case	3.47	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	100	°C/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	1000	1100		V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage TemperatureCoefficient	I_D=250μA, Referenced to25°C		0.74		V/°C
IDSS	Zero Gate Voltage Drain Current	V_{DS} =1000 V, V_{GS} = 0 V			1	μA
IDSS	Zero Gate Voltage Drain Current	V_{DS} = 720 V, TC = 125°C			10	μA
IGSSF	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
IGSSR	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V			-100	nA
VGS(TH)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D =250 uA	2.0	3.5	4.0	V
RDS(On)	Drain-Source On-state Resistance	V_{GS}=10 V, I_D =4.5 A,		8000	9600	mΩ
C_{iss}	Input Capacitance	V_{DS}=25 V, V_{GS}=0V, f=1.0 MHz		308		pF
C_{oss}	Output Capacitance			32		pF
C_{rss}	Reverse Transfer Capacitance			6.2		pF
td(on)	Turn On Delay Time	V_{DD}=500 V, ID=1.5A, R_G=25Ω		35		ns
t_r	Rising Time			12		ns
td(off)	Turn Off Delay Time			85		ns
t_f	Fall Time			53		ns
Q_g	Total Gate Charge	V_{DS}=800V, ID=1.5A, V_{GS}=15V		16		nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			11.5		nC
ISM	Maximum Pulsed Drain-Source Diode Forward Current				1.5	A
V_{SD}	Diode Forward Voltage	V_{GS}= 0 V, I_S = 9 A			1.4	V
trr	Reverse Recovery Time	V_{GS}=0V, I_S=1.5A, dI_F/dt=100 A/μs Note4)		380		ns
Q_{rr}	Reverse Recovery Charge			1.45		μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . L=20mH IAS=3A, VDD=90V, RG=25Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

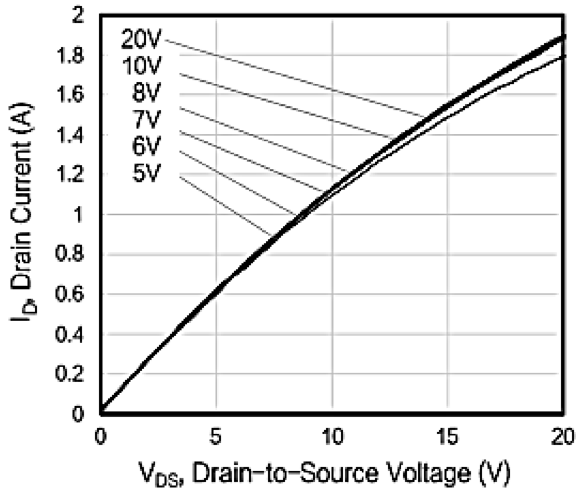


Figure 1. Output Characteristics

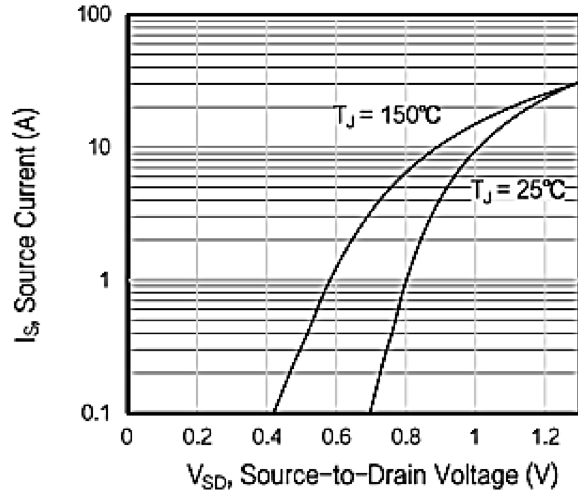


Figure 2. Body Diode Forward Voltage

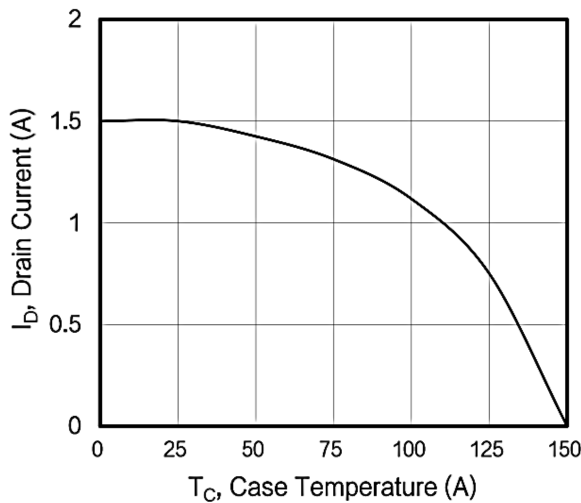


Figure3. Drain Current vs. Temperature

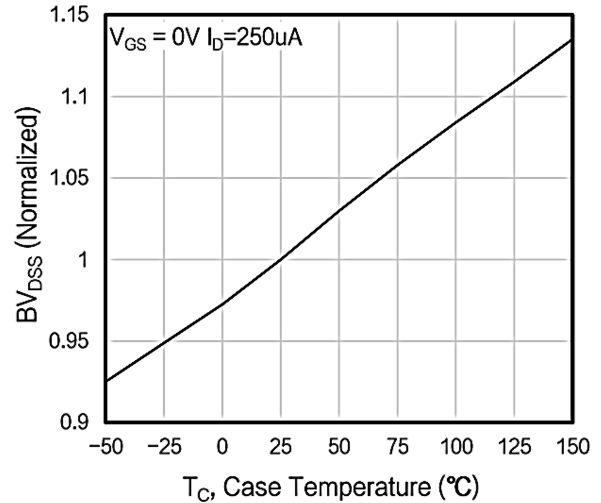


Figure4. BVDSS Variation vs. Temperature

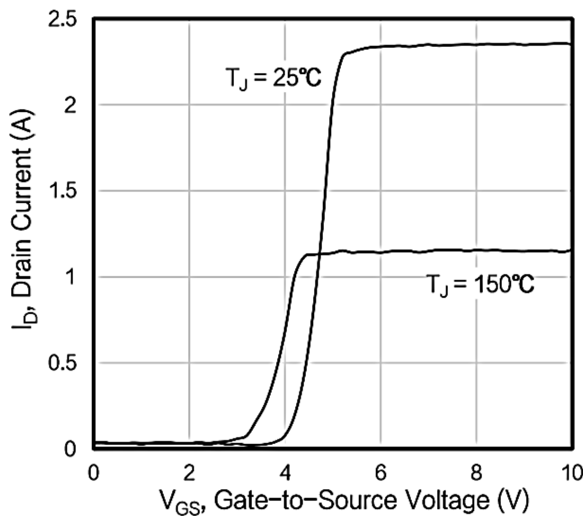


Figure 5. Transfer Characteristics

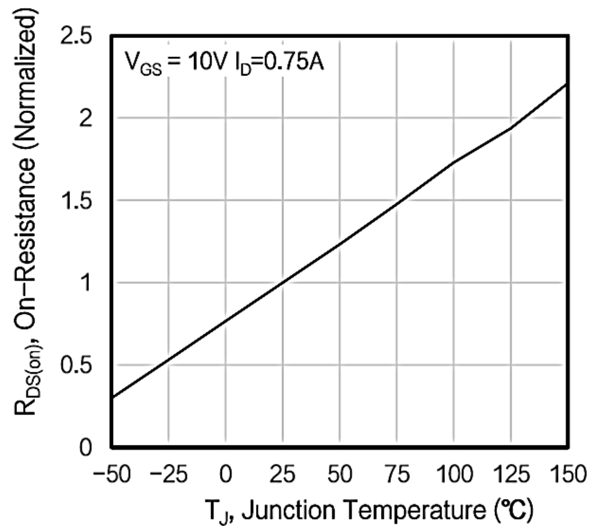


Figure 6. On-Resistance vs. Temperature

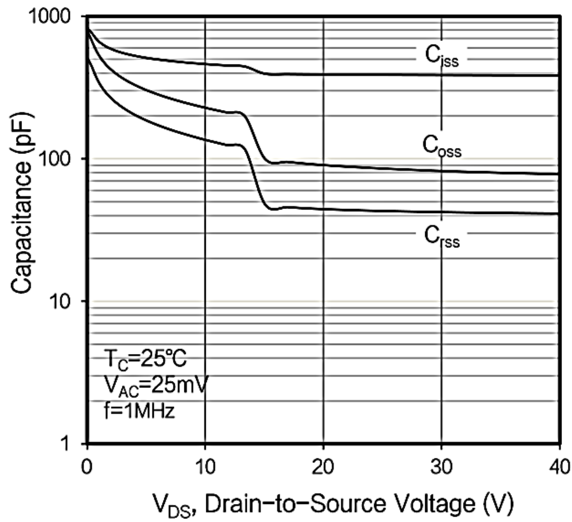


Figure 7. Capacitance

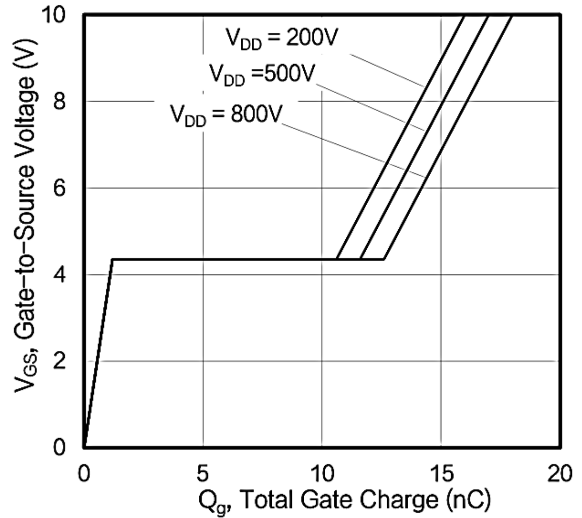


Figure 8. Gate Charge

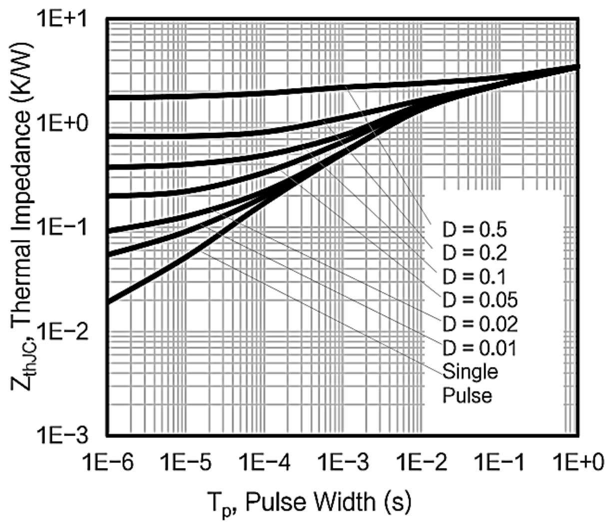
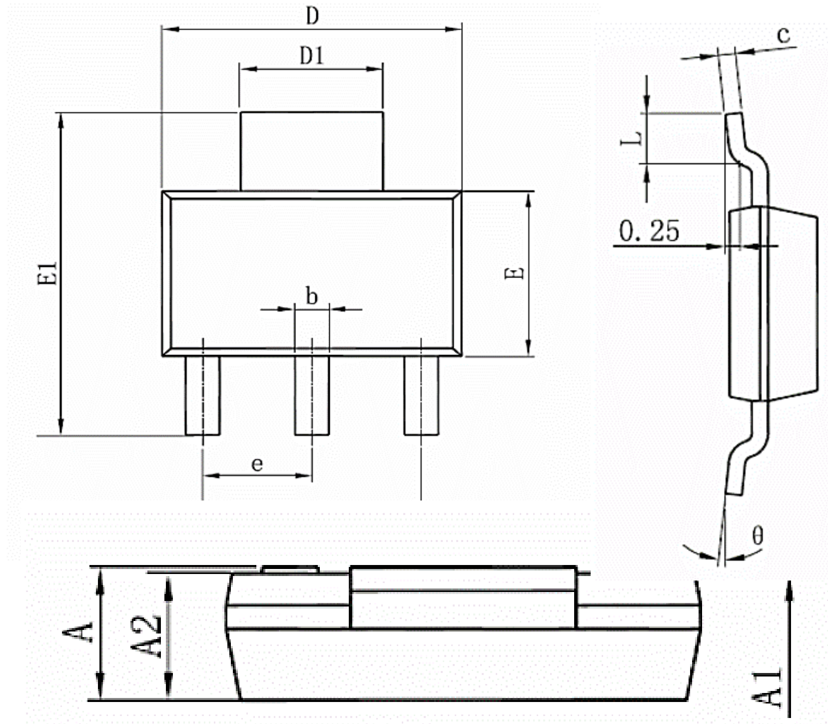


Figure 9. Transient Thermal Impedance

Package Mechanical Data:SOT223-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.52	1.8	0.06	0.049
A1	0.000	0.100	0.000	0.004
A2	1.5	1.7	0.059	0.045
b	0.66	0.82	0.026	0.032
c	0.25	0.35	0.010	0.014
D	6.2	6.4	0.244	0.252
D1	2.9	3.1	0.114	0.122
E	3.3	3.7	0.130	0.146
E1	6.83	7.07	0.269	0.278
e	2.300(BSC)		0.037(BSC)	
e1	4.500	4.700	0.177	0.185
L	0.900	1.15	0.035	0.045
θ	0°	10°	0°	10°