

650V N-SJ Enhancement Mode MOSFET

General Description

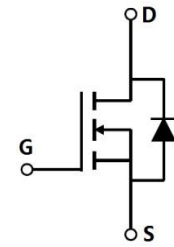
APJ15N70F use advanced Super junction MOS technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device offers extremely fast and robust body diode, and is suitable for telecom and power supplies.

Features

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Easy to drive

Applications

- Lighting
- Server power supply
- Telecom
- Solar inverter



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APJ15N70F	TO-220F-3L	APJ15N70F XXX YYYY	1000

Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	700	V
Gate source voltage	V_{GS}	± 30	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	15	A
Continuous drain current ¹⁾ , $T_C=100^\circ\text{C}$		11	
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, pulse}$	54	A
Power dissipation ³⁾ for TO220, TO262, TO263, TO247, $T_C=25^\circ\text{C}$	P_D	151	W
Power dissipation ³⁾ for TO220F, $T_C=25^\circ\text{C}$		34	
Single pulsed avalanche energy ⁵⁾	E_{AS}	272	mJ
MOSFET dv/dt ruggedness, $V_{DS}=0\dots 480\text{ V}$	dv/dt	100	V/ns
Reverse diode dv/dt, $V_{DS}=0\dots 480\text{ V}$, $I_{SD}\leq I_D$	dv/dt	50	V/ns
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ\text{C}$

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Thermal resistance, junction-case	$R_{\theta JC}$	3.68	$^{\circ}\text{C/W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$

Electrical Characteristics at $T_j=25^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	650			V	$V_{GS}=0\text{ V}, I_D=250\ \mu\text{A}$
		700	770			$V_{GS}=0\text{ V}, I_D=250\ \mu\text{A}, T_j=150^{\circ}\text{C}$
Gate threshold voltage	$V_{GS(th)}$	3.5		4.5	V	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$
Drain-source on-state resistance	$R_{DS(on)}$		0.18	0.22	Ω	$V_{GS}=10\text{ V}, I_D=9\text{ A}$
			0.45			$V_{GS}=10\text{ V}, I_D=9\text{ A}, T_j=150^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=30\text{ V}$
				-100		$V_{GS}=-30\text{ V}$
Drain-source leakage current	I_{DSS}			10	μA	$V_{DS}=650\text{ V}, V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		1493		pF	$V_{GS}=0\text{ V}, V_{DS}=50$
Output capacitance	C_{oss}		101		pF	V,
Reverse transfer capacitance	C_{rss}		2.05		pF	$f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$		45.28		ns	$V_{GS}=10\text{ V},$
Rise time	t_r		82.64		ns	$V_{DS}=400\text{ V},$
Turn-off delay time	$t_{d(off)}$		42.20		ns	$R_G=20\ \Omega,$
Fall time	t_f		32.56		ns	$I_D=18\text{ A}$
Total gate charge	Q_g		21.7		nC	$I_D=18\text{ A},$
Gate-source charge	Q_{gs}		8.04		nC	$V_{DS}=400\text{ V},$
Gate-drain charge	Q_{gd}		7.4		nC	$V_{GS}=10\text{ V}$
Gate plateau voltage	$V_{plateau}$		7.2		V	
Diode forward current	I_S			18	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			54	A	
Diode forward voltage	V_{SD}			1.2	V	$I_S=18\text{ A}, V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		143.3		ns	$V_R=400\text{ V}, I_S=18\text{ A}, di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		767		nC	
Peak reverse recovery current	I_{rrm}		10.7		A	

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating, pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25^{\circ}\text{C}$.
- 5) $V_{DD}=100\text{ V}, R_G=25\ \Omega, L=10\text{ mH}$, starting $T_j=25^{\circ}\text{C}$.

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Electrical Characteristics Diagrams

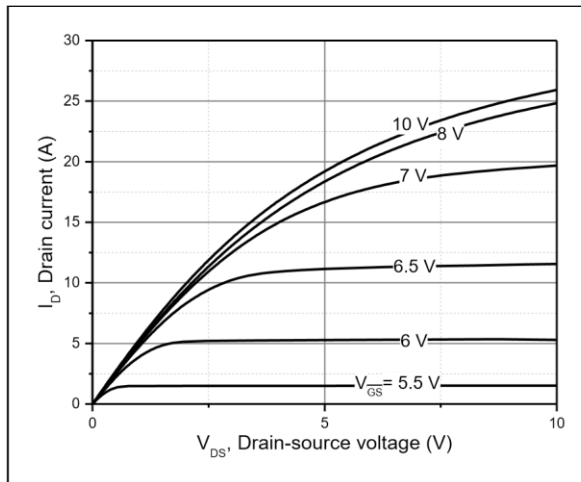


Figure 1, Typ. output characteristics

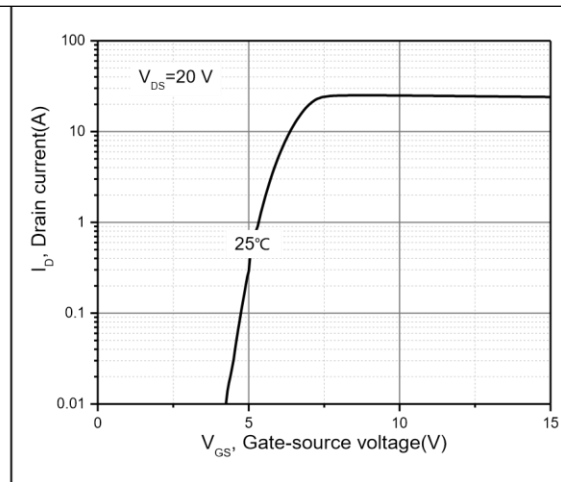


Figure 2, Typ. transfer characteristics

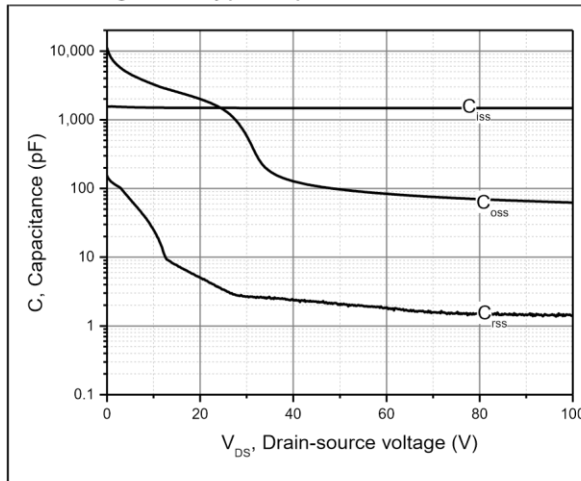


Figure 3, Typ. capacitances

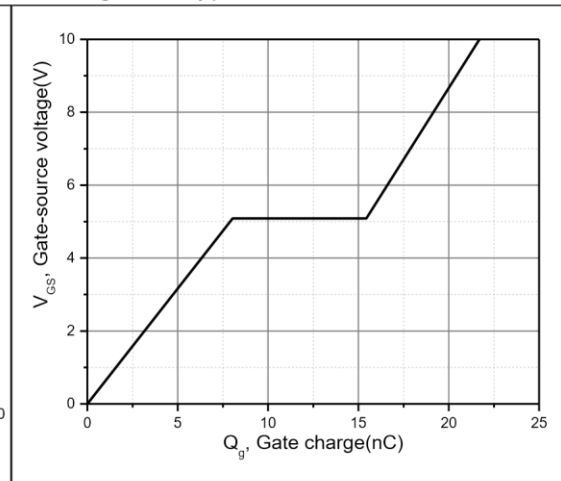


Figure 4, Typ. gate charge

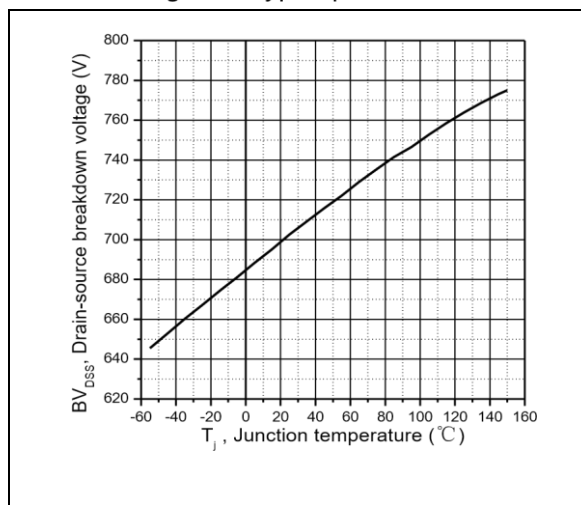


Figure 5, Drain-source breakdown voltage

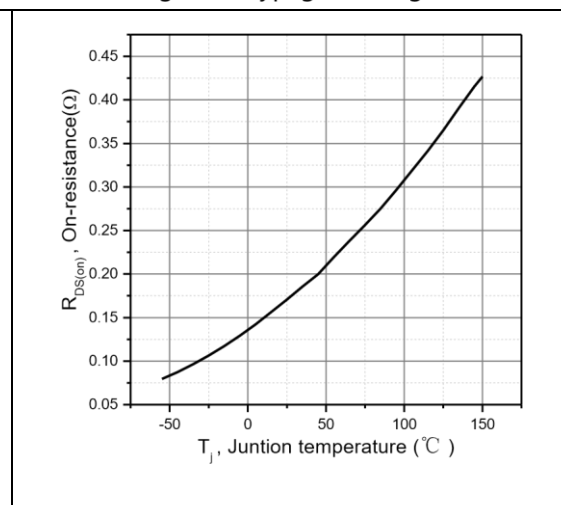


Figure 6, Drain-source on-state resistance

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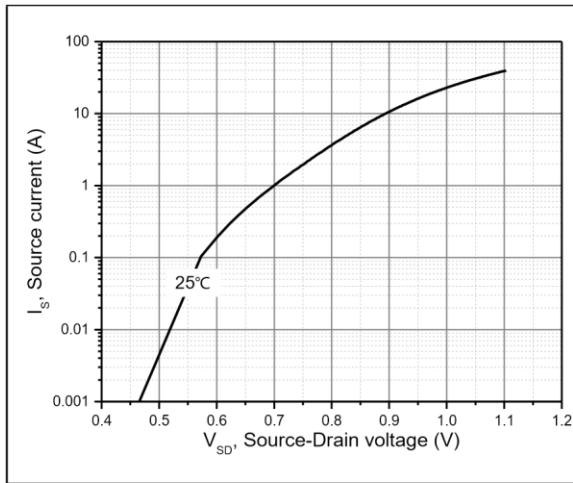


Figure 7, Forward characteristic of body diode

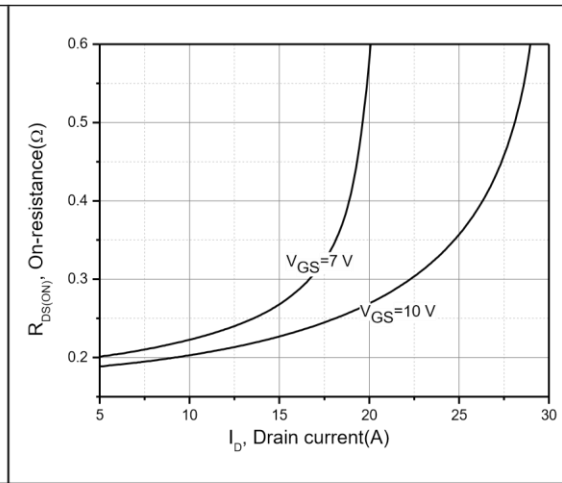


Figure 8, Drain-source on-state resistance

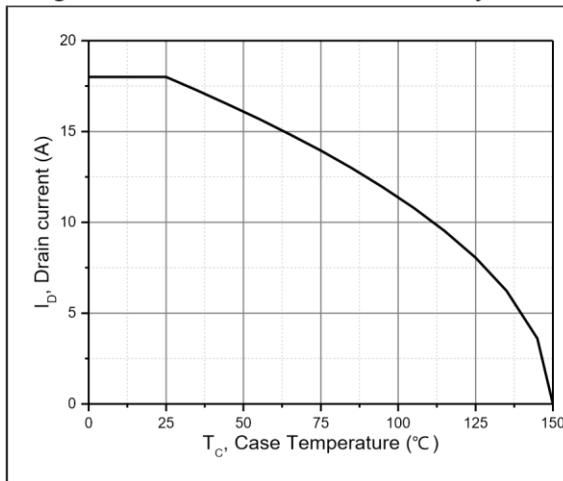


Figure 9, Drain current

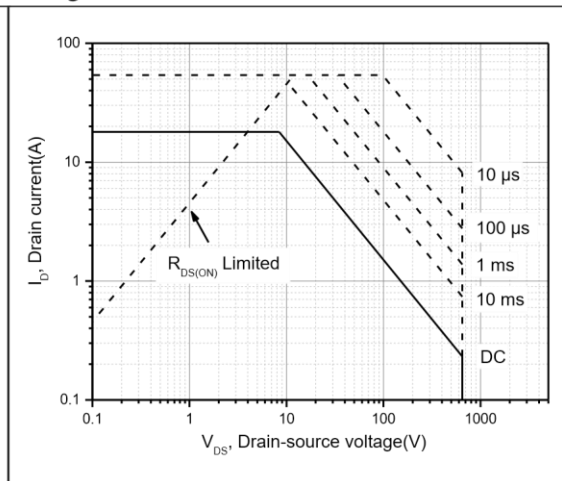


Figure 10, Safe operation area for TO220/TO262/TO263/TO247 $T_C=25\text{ }^\circ\text{C}$

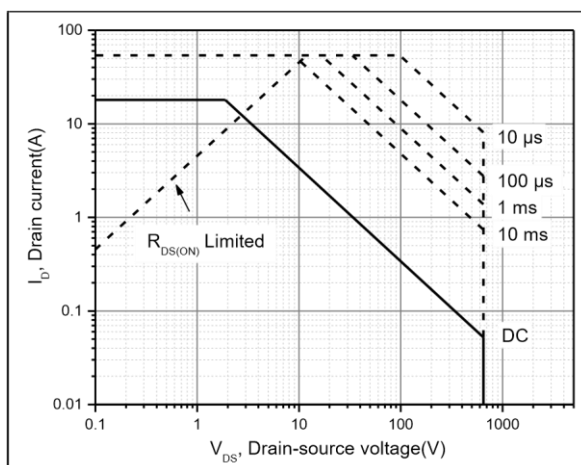


Figure 11, Safe operation area for TO220F $T_C=25\text{ }^\circ\text{C}$

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Test circuits and waveforms

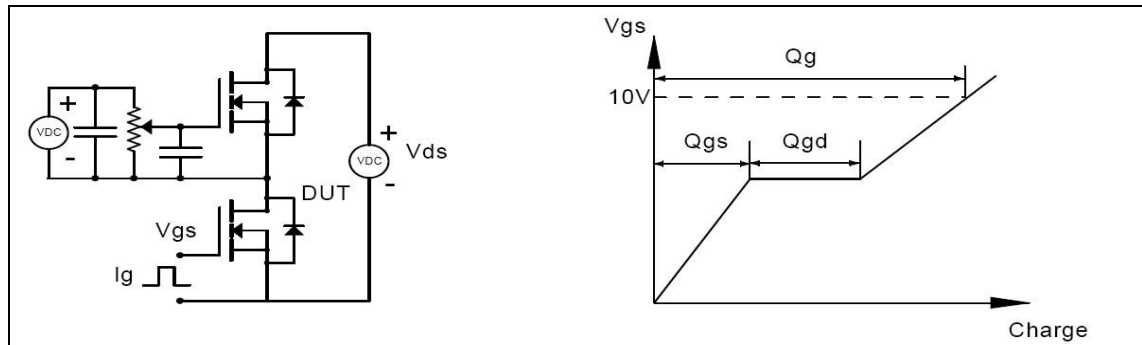


Figure 1, Gate charge test circuit & waveform

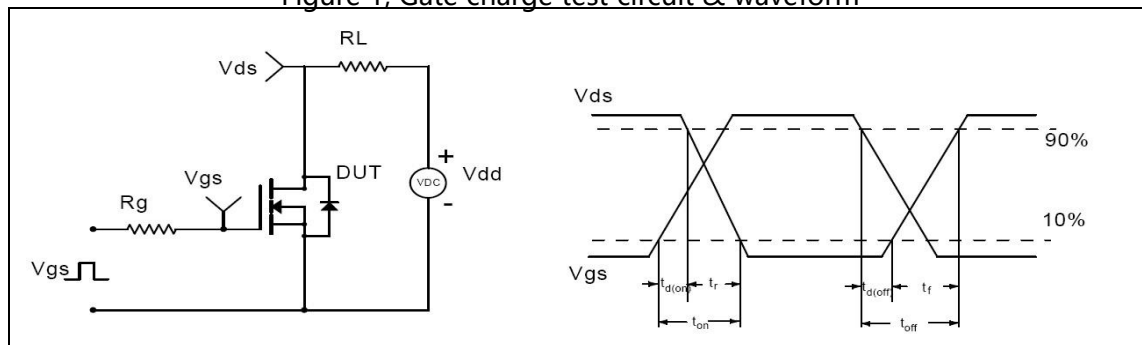


Figure 2, Switching time test circuit & waveforms

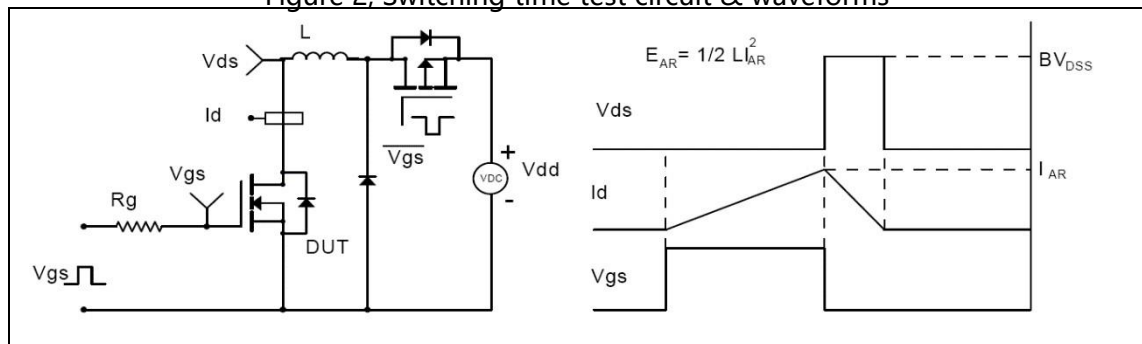


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

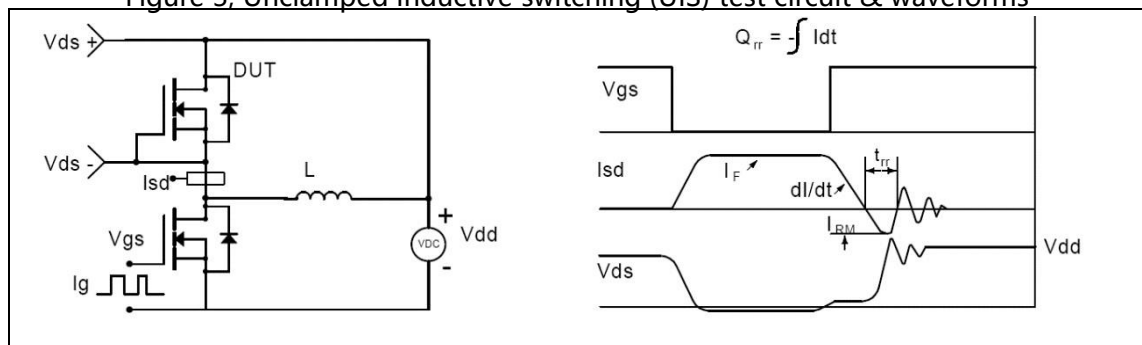


Figure 4, Diode reverse recovery test circuit & waveforms

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