

650V N-Channel Enhancement Mode MOSFET

Description

The APJ150N60MP is **CoolFET II** MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance. APJ150N60MP is suitable for applications which require superior power density and outstanding efficiency

General Features

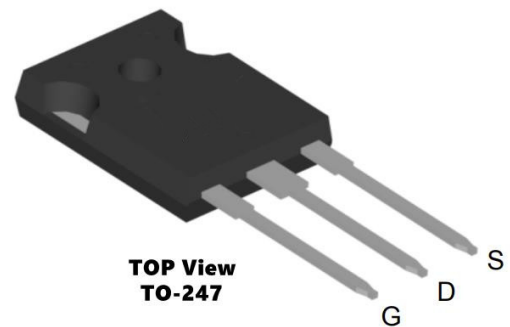
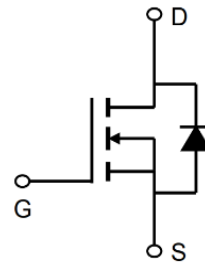
$V_{DS} = 600V$ (Type: 680V) $IDM = 150A$

$R_{DS(ON)} < 70m\Omega$ @ $V_{GS}=10V$ (Type: **62mΩ**)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APJ150N60MP	TO-247-3L	APJ150N60MP XXX YYYY	300

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	600	V
I_D	Continuous Drain Current	48	A
I_{DM}	Pulsed Drain Current (note1)	150	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	550	mJ
P_{tot}	Power Dissipation ($T_c = 25^\circ C$)	500	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	0.25	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62	$^\circ C/W$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =1mA	600	680	-	V
V(GS)th	Gate threshold voltage	V _{DS} =V _{GS} , I _D =1mA	3	4	5	V
I _{DSS}	Zero gate voltage drain current	V _{DS} =600V, V _{GS} =0V, T _J =25°C	-	-	10	μA
I _{GSS}	Gate-source leakage current	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
R _{DS(on)}	Drain-source on-state resistance	V _{GS} =10V, I _D =23.5A, T _J =25°C	-	62	70	mΩ
R _G	Gate resistance	V _{DD} =0V, V _{GS} =0V, F=1MHz	-	3.6	-	Ω
C _{iss}	Input capacitance	V _{GS} =0V, V _{DS} =50V, f=250kHz	-	3750	-	pF
C _{oss}	Output capacitance		-	110	-	pF
C _{rss}	Reverse transfer capacitance		-	4	-	pF
t _{d(on)}	Turn-on delay time	V _{DD} =400V, V _{GS} =10V, I _D =23A	-	87	-	ns
t _r	Rise time		-	66	-	ns
t _{d(off)}	Turn-off delay time		-	125	-	ns
t _f	Fall time		-	72	-	ns
Q _{gs}	Gate to source charge	V _{DD} =400V, I _D =23A, V _{GS} =0 to 10V	-	20	-	nC
Q _{gd}	Gate to drain charge		-	16	-	nC
Q _g	Gate charge total		-	70	-	nC
V _{plateau}	Gate plateau voltage	V _{DD} =400V, I _D =23A, V _{GS} =0 to 10V	-	5.3	-	V
V _{SD}	Diode forward voltage	V _{GS} =0V, I _F =23A, T _r =25°C	-	0.88	-	V
t _{rr}	Reverse recovery time	V _R =100V, I _F =23A, di _F /dt=100A/μs	-	147	-	ns
Q _{rr}	Reverse recovery charge		-	1.32	-	μC
I _{rrm}	Peak reverse recovery current		-	17	-	A

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The EAS data shows Max. rating . L=0.5mH, I_{AS} =7A, V_{DD} =50V, R_G=25Ω
3. The test condition is Pulse Test: I_{SD} ≤ I_D, di/dt = 100A/μs, V_{DD} ≤ BVDSS, Starting at T_J =25°C
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics

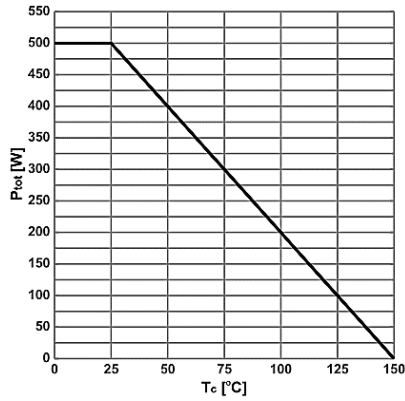


Figure1: Power dissipation (Non FullPAK)

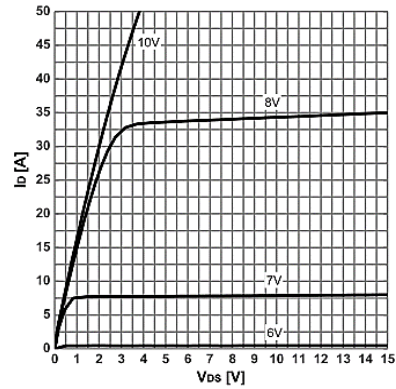


Figure2: output characteristics

$I_D=f(V_{DS}); T_j=25^{\circ}\text{C}; \text{parameter: } V_{GS}$

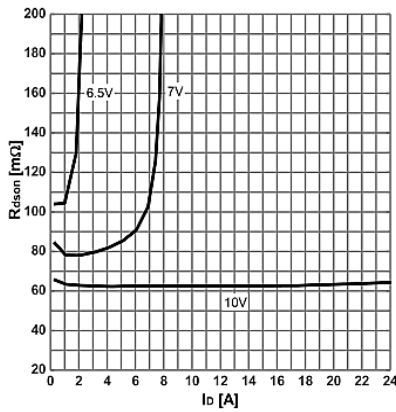


Figure3: Typ. drain-source on-state resistance

$R_{DS(on)}=f(I_D); T_j=25^{\circ}\text{C}; \text{parameter: } V_{GS}$

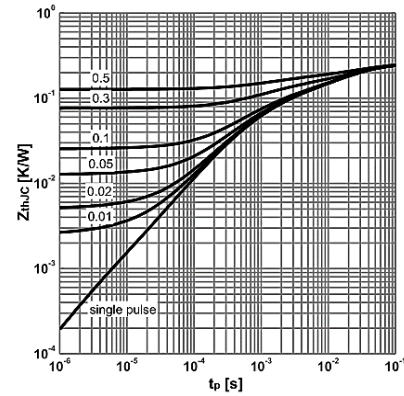


Figure4:Max. transient thermal impedance

$P_{tot}=f(T_C)$

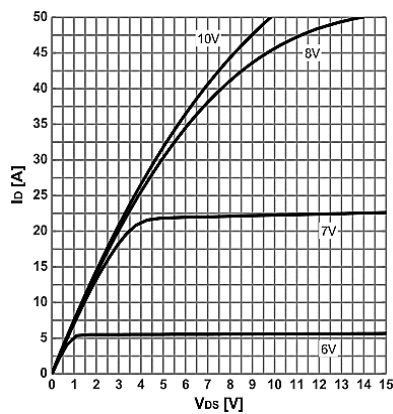


Figure5: Type. output characteristics
 $I_D=f(V_{DS}); T_j=125^{\circ}\text{C}; \text{parameter: } V_{GS}$

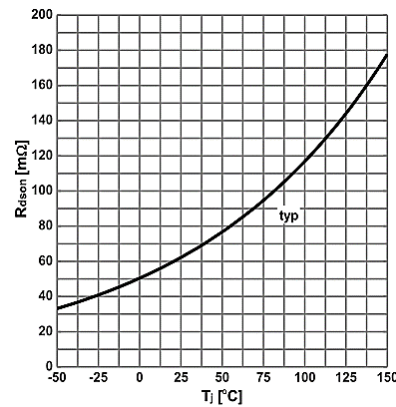


Figure6: Max. transient thermal impedance
 $R_{DS(on)}=f(T_j); I_D=23.5\text{A}; V_{GS}=10\text{V}$

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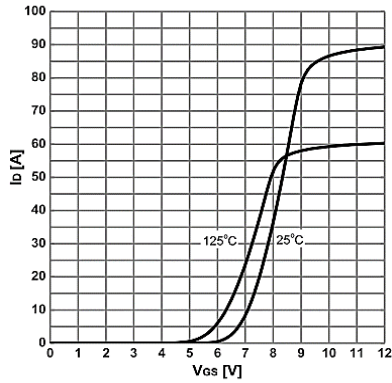


Figure 7: Typ. transfer characteristics

$I_D=f(V_{GS})$; $V_{DS}=20V$; parameter: T_j

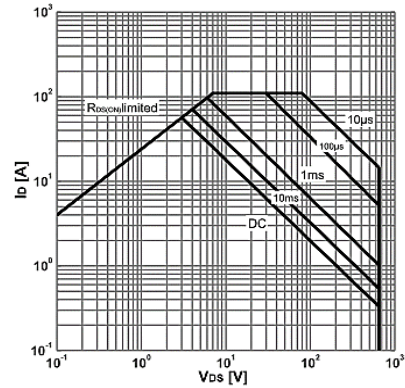


Figure 8 : Safe operating area (Non FullPAK)

$I_D=f(V_{DS})$; $T_j=25^\circ C$; $D=0$; parameter: t_p

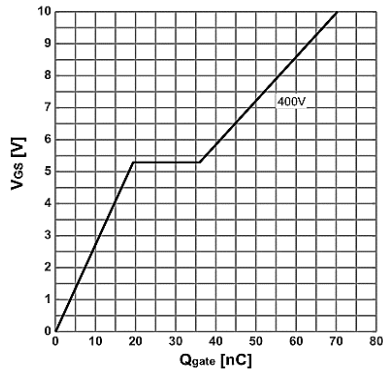


Figure9: Typ. gate charge

$V_{GS}=f(Q_{gate})$; $I_D=25A$ pulsed; $V_{DS}=400V$

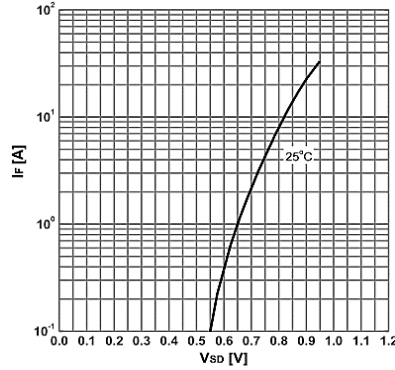


Figure 10: Forward characteristics of reverse diode

$I_F=f(V_{SD})$; parameter: T_j

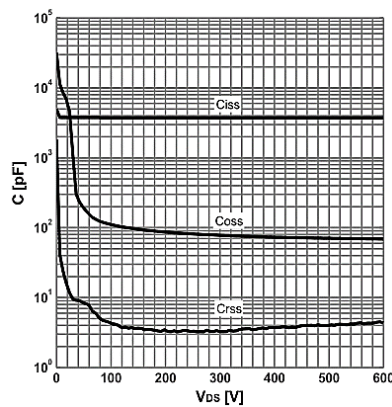


Figure 11: Typ. capacitances

$C=f(V_{DS})$; $V_{GS}=0V$; $f=250kHz$

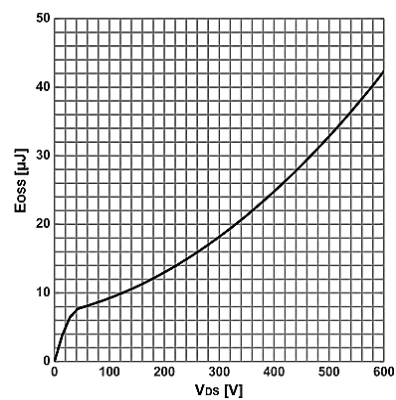
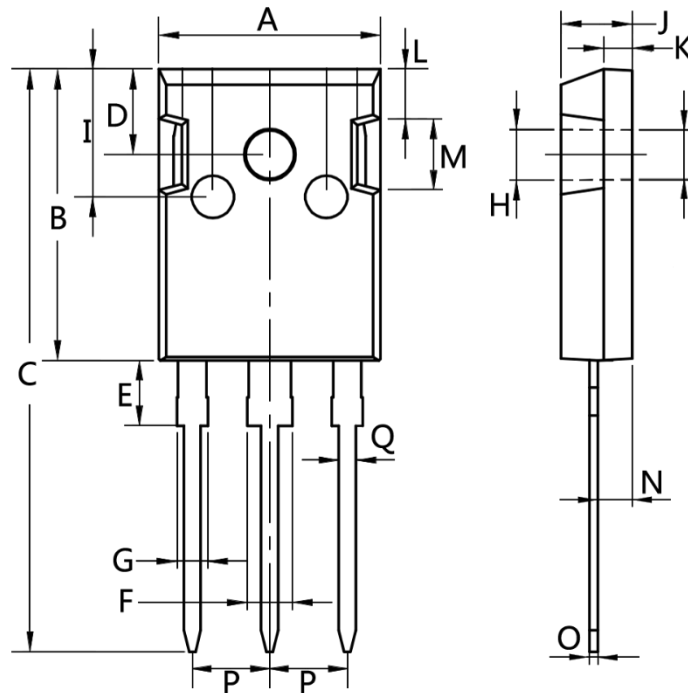


Figure 12: Typ. Coss stored energy

$E_{OSS}=f(V_{DS})$

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Package Mechanical Data-TO-247-3L


Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3