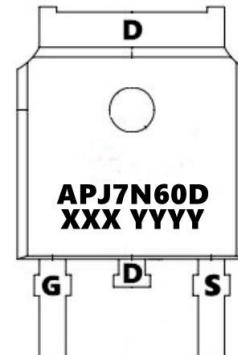
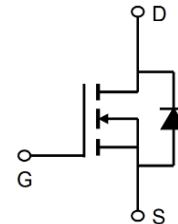


600V N-Channel Enhancement Mode MOSFET
Description

The APJ7N60F/P/T is **CoolFET III** MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance. APJ7N60D is suitable for applications which require superior power density and outstanding efficiency


General Features

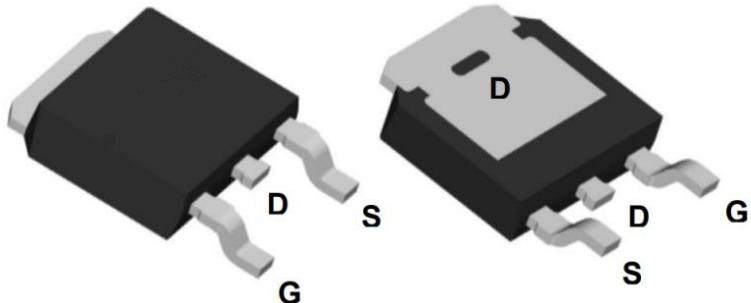
$V_{DS} = 600V$ (Type: 640V) $IDM = 7A$

$R_{DS(ON)} < 1200m\Omega$ @ $V_{GS}=10V$ (**Type: 1100m Ω**)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)


Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APJ7N60D	TO-252-3L	APJ7N65D XXX YYYY	2500

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$VDSS$	Drain-Source Voltage ($V_{GS} = 0V$)	600	V
ID	Continuous Drain Current	4	A
IDM	Pulsed Drain Current (note1)	7	A
VGS	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	130	mJ
P_D	Power Dissipation ($T_c = 25^\circ C$)	28.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55~+150	°C
R_{thJC}	Thermal Resistance, Junction-to-Case	4.4	°C/W
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62	°C/W



600V N-Channel Enhancement Mode MOSFET
Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	600	640	--	V
$\Delta V_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=250\mu\text{A}$, referenced to 25°C	--	0.7	--	$\text{V}/^\circ\text{C}$
IDSS	Drain to source leakage current	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$	--	--	1	μA
		$V_{DS}=400\text{V}$, $T_C=125^\circ\text{C}$	--	--	50	μA
IGSS	Gate to source leakage current, forward	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$	--	--	100	nA
	Gate to source leakage current, reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$	--	--	-100	nA
VGS(TH)	Gate threshold voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5	3.0	4.5	V
RDS(ON)	Drain to source on state resistance	$V_{GS}=10\text{V}$, $I_D=2\text{A}$	--	1100	1200	$\text{m}\Omega$
Ciss	Input capacitance	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$	--	280	--	pF
Coss	Output capacitance		--	26	--	
Crss	Reverse transfer capacitance		--	2.3	--	
td(on)	Turn on delay time	$V_{DS}=480\text{V}$, $I_D=4\text{A}$, $R_G=20\Omega$, $V_{GS}=10\text{V}$	--	6.	--	ns
tr	Rising time		--	3	--	
td(off)	Turn off delay time		--	48	--	
tf	Fall time		--	8	--	
Qg	Total gate charge	$V_{DS}=480\text{V}$, $V_{GS}=10\text{V}$, $I_D=4\text{A}$	--	2.77	--	nC
Qgs	Gate-source charge		--	5.8	--	
Qgd	Gate-drain charge		--	20.4	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	14	A
ISM	Pulsed source current		--	--	44	A
VSD	Diode forward voltage drop.	$I_S=4\text{A}$, $V_{GS}=0\text{V}$	--	0.7	1.5	V
Tr	Reverse recovery time	$I_S=4\text{A}$, $V_{GS}=0\text{V}$, $V_{DD}=400\text{V}$, $dI_F/dt=100\text{A/us}$,	--	218	--	ns
Qrr	Reverse recovery Charge		--	6.5	--	uC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . L=0.5mH, IAS =2A, VDD =50V, RG=25Ω
- 3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at $T_J = 25^\circ\text{C}$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

600V N-Channel Enhancement Mode MOSFET

Typical Characteristics

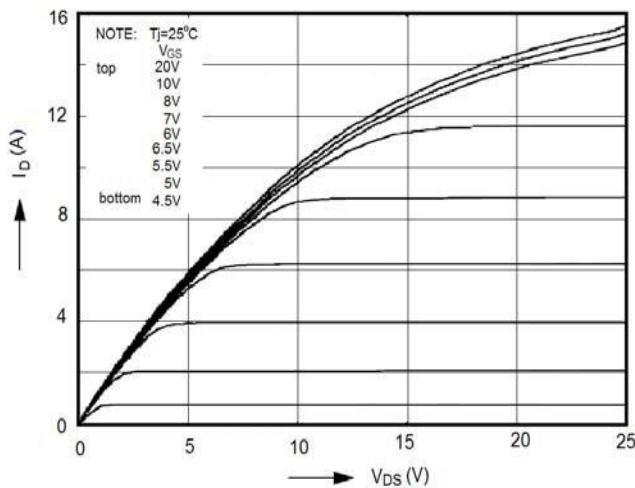


Figure1. Typical Output Characteristics

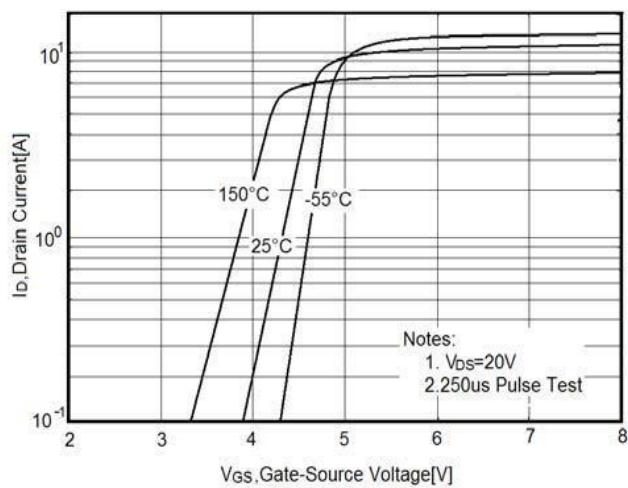


Figure2. Typical Transfer Characteristics

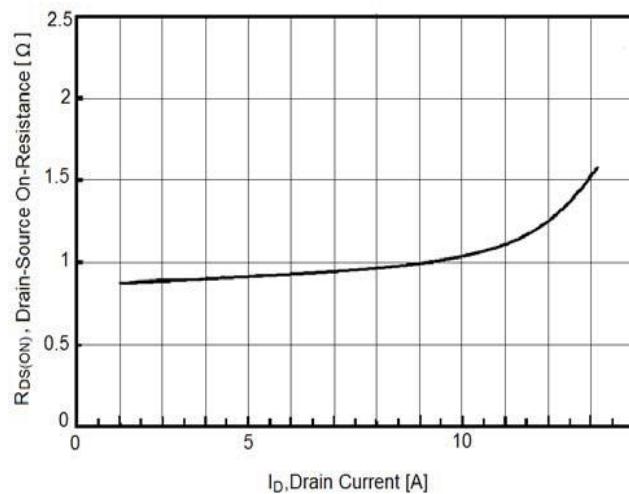


Figure3. $R_{DS(on)}$ vs I_D

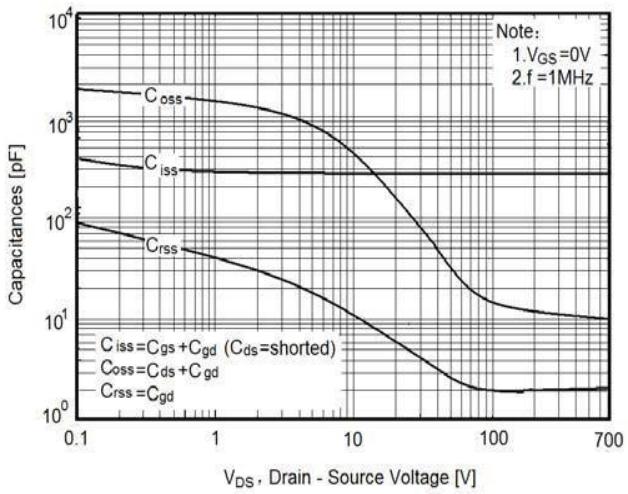


Figure4. Capacitance vs V_{DS}

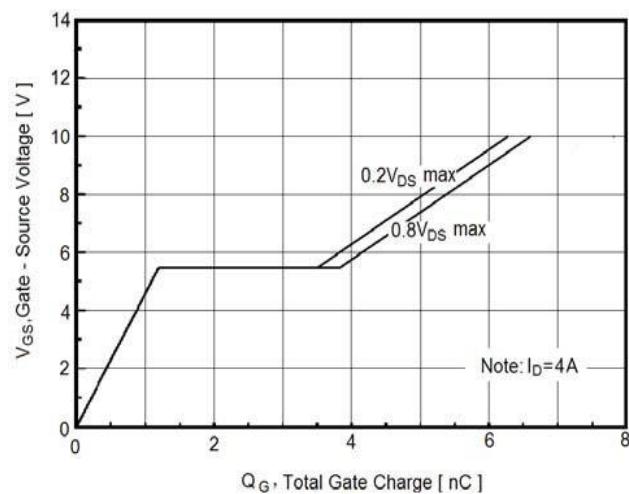


Figure5. Gate Charge Characteristics

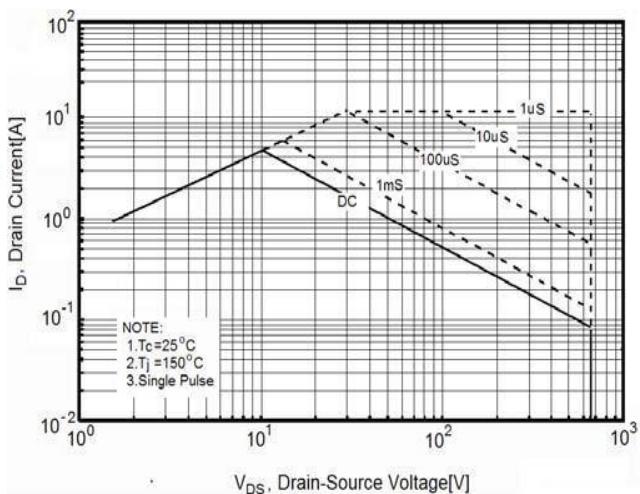


Figure6. Maximum Forward Biased Safe Operating Area



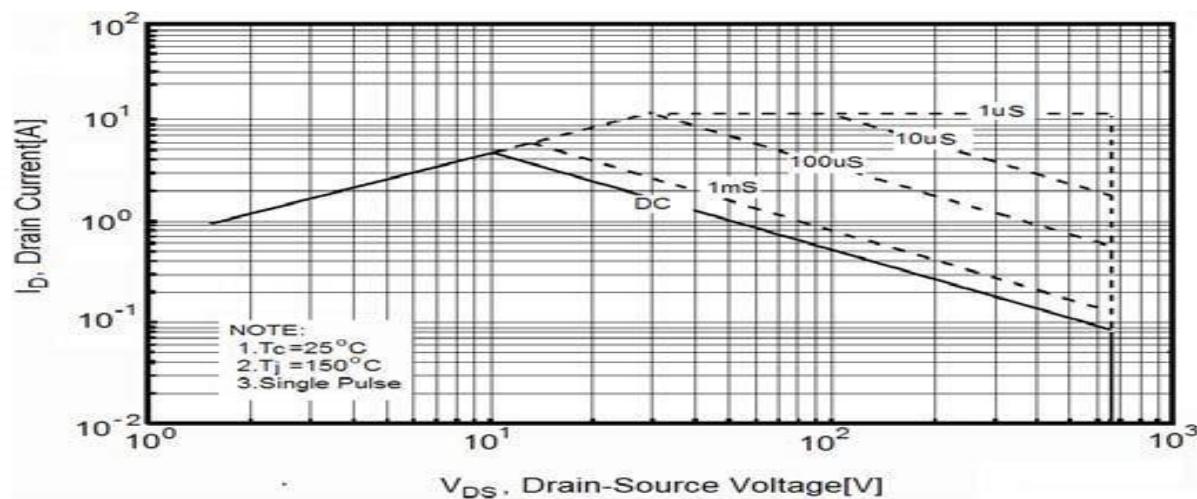
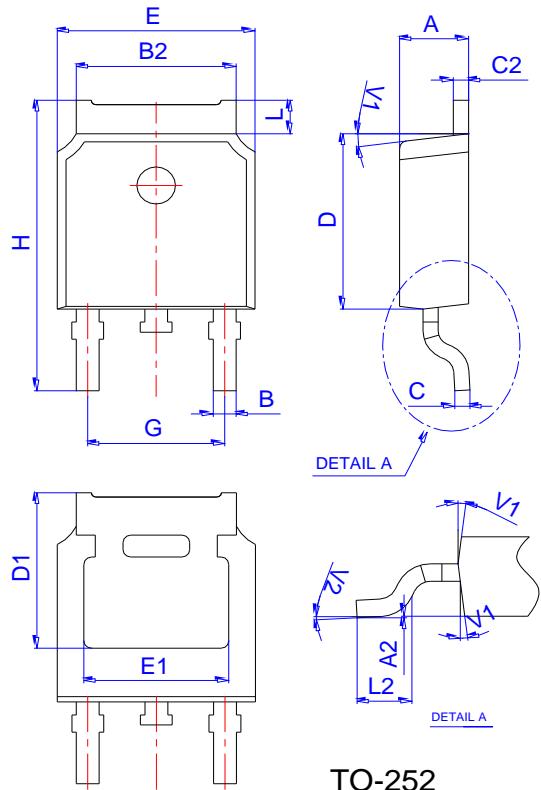
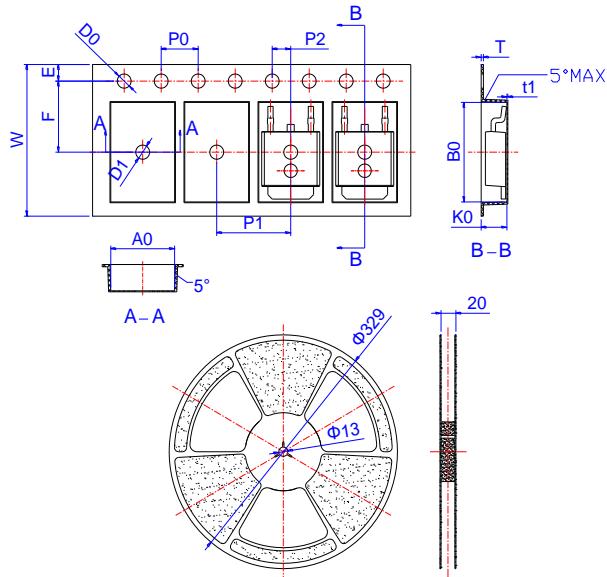


Figure7. Normalized Thermal Response

Figure 12: Type. gate charge

600V N-Channel Enhancement Mode MOSFET
Package Mechanical Data: TO-252-3L

TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10			2.50	0.083	
A2	0			0.10	0	
B	0.66			0.86	0.026	
B2	5.18			5.48	0.202	
C	0.40			0.60	0.016	
C2	0.44			0.58	0.017	
D	5.90			6.30	0.232	
D1	5.30REF			0.209REF		
E	6.40			6.80	0.252	
E1	4.63				0.182	
G	4.47			4.67	0.176	
H	9.50			10.70	0.374	
L	1.09			1.21	0.043	
L2	1.35			1.65	0.053	
V1		7°				7°
V2	0°			6°	0°	
						6°

Reel Specification-TO-252


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583