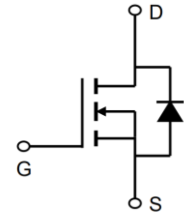
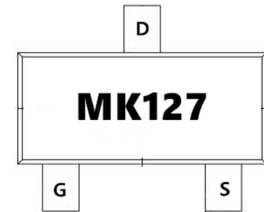
# AP01N60AI

## 600V N-Channel Enhancement Mode MOSFET




### Description

The AP01N60AI is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

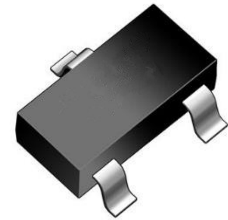



### General Features

VDS =600V,ID =100mA

RDS(ON) <300Ω@ VGS=10V

### Application



Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)

### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP01N60AI | SOT-23 | MK127 | 3000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 600 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_A$=25℃ | Drain Current[3], $V_{GS}$ @ 10V | 100 | mA |
| $I_D$@$T_A$=70℃ | Drain Current[3], $V_{GS}$ @ 10V | 21 | mA |
| $I_{DM}$ | Pulsed Drain Current[1] | 150 | mA |
| $P_D$@$T_A$=25℃ | Total Power Dissipation | 0.5 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| Rthj-a | Maximum Thermal Resistance, Junction-ambient[3] | 250 | ℃/W |

## Electrical Characteristics ($T_A$=25℃unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250uA | 600 | 650 | - | V |
| RDS(ON) | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V, $I_D$=16mA | - | 80 | 300 | Ω |
| VGS(th) | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250uA | 2 | 2.3 | 4 | V |
| $g_{fs}$ | Forward Transconductance | $V_{DS}$=10V, $I_D$=16mA | - | 28 | - | mS |
| IDSS | Drain-Source Leakage Current | $V_{DS}$=480V, $V_{GS}$=0V | - | - | 25 | uA |
| IGSS | Gate-Source Leakage | $V_{GS}$=$\pm$20V, $V_{DS}$=0V | - | - | $\pm$100 | nA |
| $Q_g$ | Total Gate Charge[2] | $I_D$=0.1A<br>$V_{DS}$=200V<br>$V_{GS}$=10V | 1.8 | 2.5 | 3.2 | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 1.3 | - | nC |
| $Q_{gd}$ | Gate-Drain ("Miller") Charge | | - | 0.8 | - | nC |
| td(on) | Turn-on Delay Time[2] | $V_{DS}$=300V $I_D$=10mA<br>$R_G$=3.3Ω,$V_{GS}$=10V<br>$R_D$=30kΩ | - | 11.5 | - | ns |
| $t_r$ | Rise Time | | - | 14.5 | - | ns |
| td(off) | Turn-off Delay Time | | - | 14 | - | ns |
| $t_f$ | Fall Time | | - | 120 | - | ns |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=V $V_{DS}$=25V<br>f=1.0MHz | 8.8 | 12.5 | 16.2 | pF |
| $C_{oss}$ | Output Capacitance | | 7 | 10 | 13 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 5 | 7 | 9 | pF |
| $V_{SD}$ | Forward On Voltage[2] | $I_S$=0.05A, $V_{GS}$=0V | - | - | 1.5 | V |

**Notes:**

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Mounted on min. copper pad.

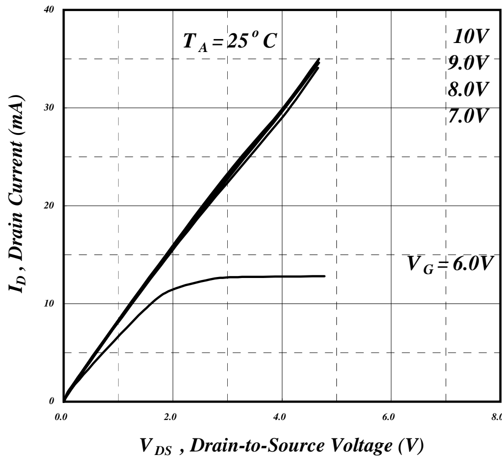



Fig 1. Typical Output Characteristics

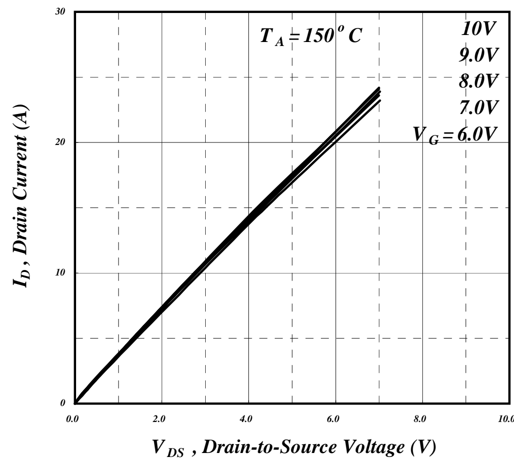



Fig 2. Typical Output Characteristics

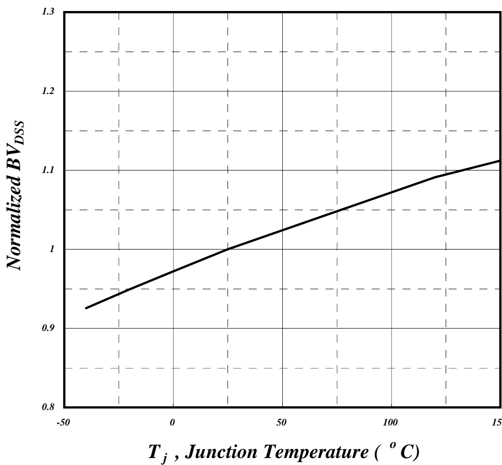



Fig 3. Normalized $BV_{DSS}$ v.s. Junction Temperature

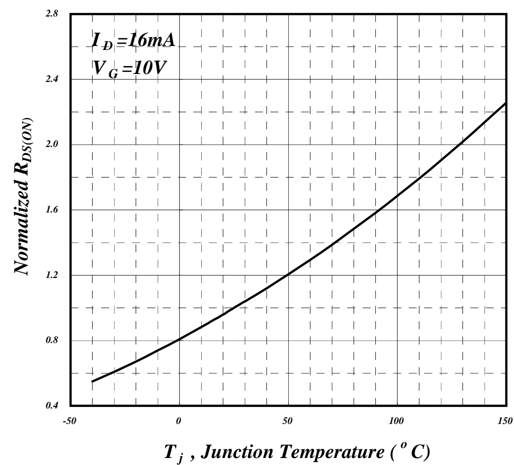



Fig 4. Normalized On-Resistance v.s. Junction Temperature

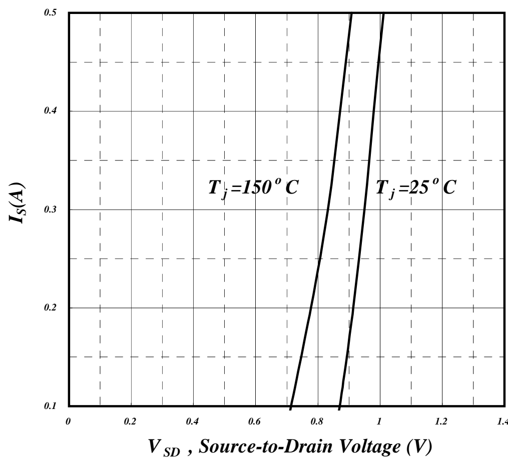



Fig 5. Forward Characteristic of Reverse Diode

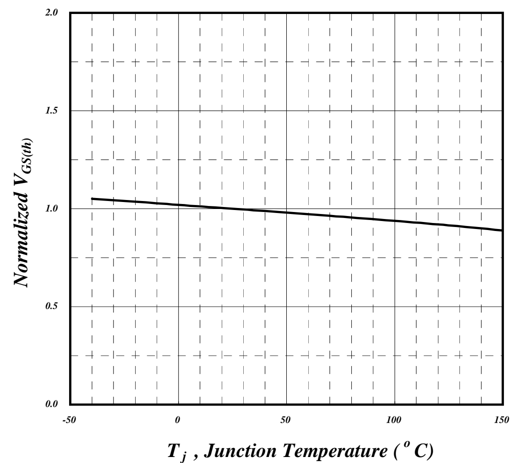



Fig 6. Gate Threshold Voltage v.s. Junction Temperature

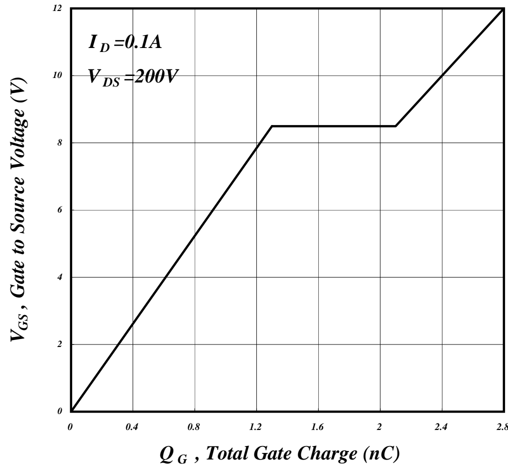



Fig 7. Gate Charge Characteristics

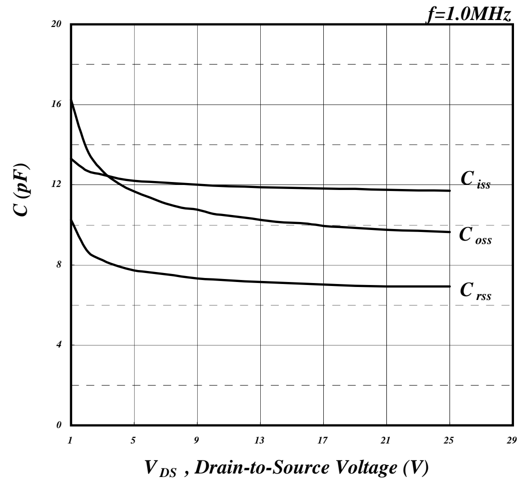



Fig 8. Typical Capacitance Characteristics

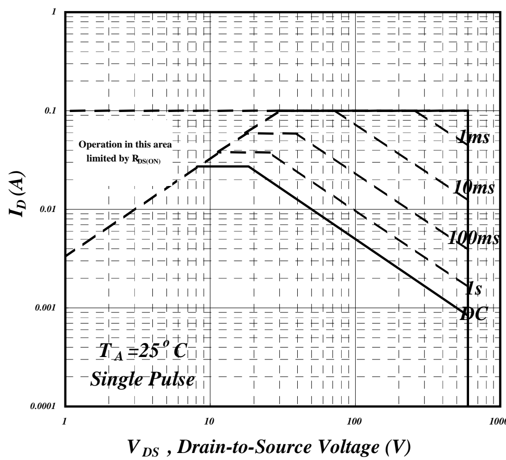



Fig 9. Maximum Safe Operating Area

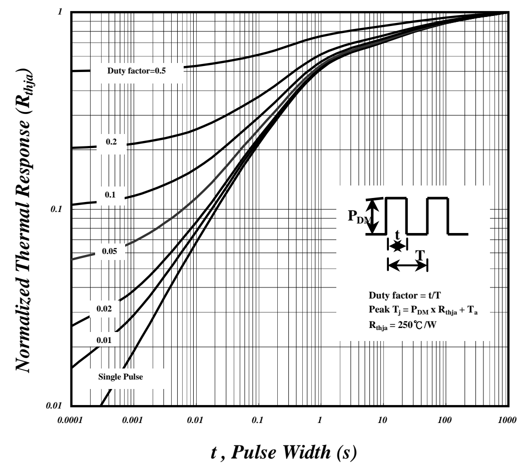
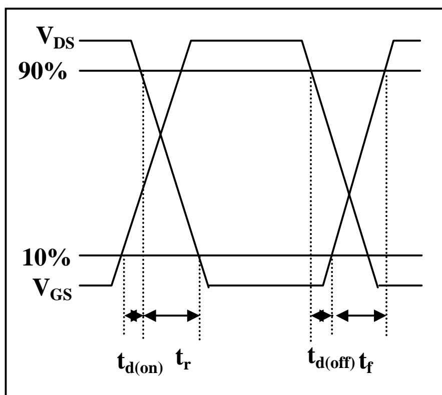



Fig 10. Effective Transient Thermal Impedance



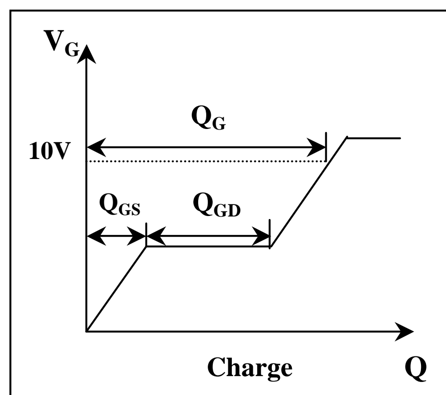
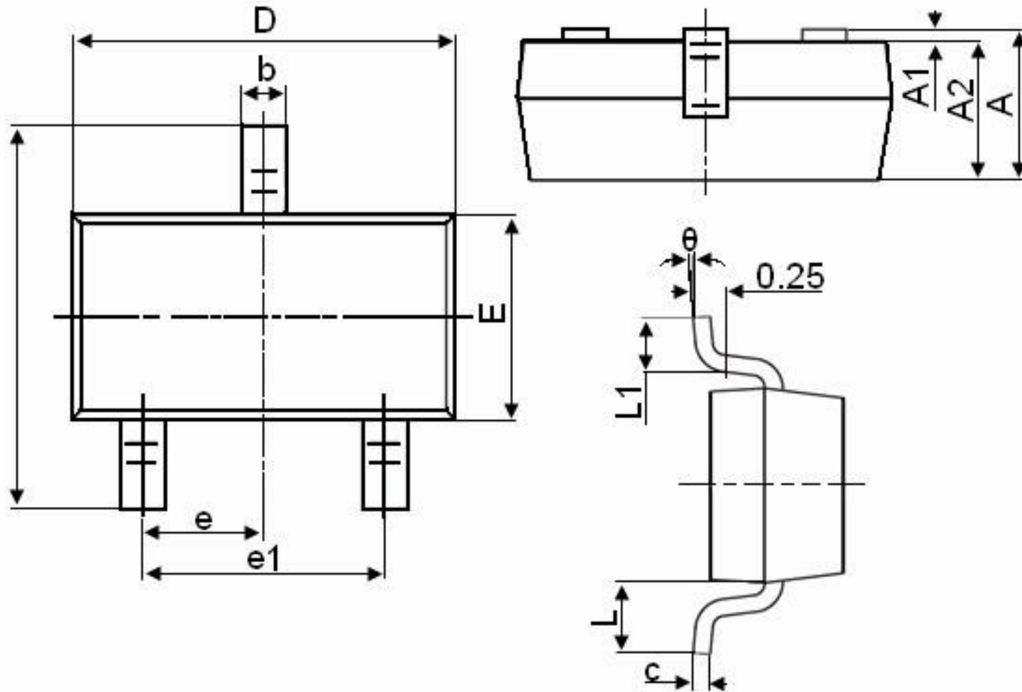




Fig 11. Switching Time Waveform

Fig 12. Gate Charge Circuit

## Package Mechanical Data-SOT23




| Symbol | Dimensions in Millimeters | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.900 | 1.150 |
| A1 | 0.000 | 0.100 |
| A2 | 0.900 | 1.050 |
| b | 0.300 | 0.500 |
| c | 0.080 | 0.150 |
| D | 2.800 | 3.000 |
| E | 1.200 | 1.400 |
| E1 | 2.250 | 2.550 |
| e | 0.950TYP | |
| e1 | 1.800 | 2.000 |
| L | 0.550REF | |
| L1 | 0.300 | 0.500 |
| θ | 0° | 8° |