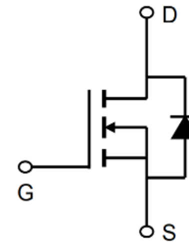
AP3N20SI

180V N-Channel Enhancement Mode MOSFET

Description

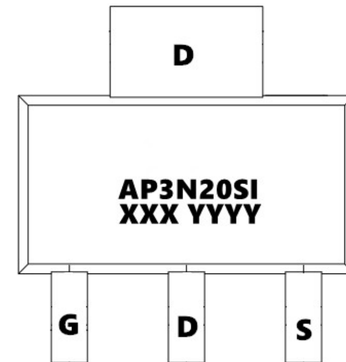
The AP3N20SI is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

V_{DS} = 180V I_D =3A

$R_{DS(ON)}$ < 1800mΩ @ V_{GS}=10V （Type：1300mΩ）

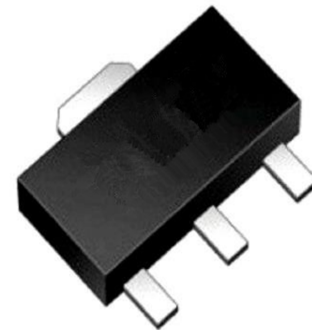


Application

Automative lighting

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3N20SI	SOT89-3L	AP3N20SI XXX YYYY	3000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	180	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	3.0	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	2.1	A
IDM	Pulsed Drain Current[1]	10	A
P_D@T_C=25℃	Total Power Dissipation	2	W
P_D@T_A=25℃	Total Power Dissipation[3]	1.1	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Maximum Thermal Resistance, Junctionambient	85	℃/W
RθJC	Maximum Thermal Resistance, Junction-case	40	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	180	195	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=200V,V_{GS}=0V	-	-	1	μA
IGSS	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	1.7	3.0	V
RDS(ON)	Drain-Source On-State Resistance	V_{GS}=10V, I_D=2A	-	1300	1800	mΩ
gFS	Forward Transconductance	V_{DS}=15V,I_D=2A	-	8	-	S
C_{Iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	580	-	PF
Coss	Output Capacitance		-	90	-	PF
C_{rss}	Reverse Transfer Capacitance		-	3	-	PF
td(on)	Turn-on Delay Time	V_{DD}=100V, R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	10	-	nS
t_r	Turn-on Rise Time		-	12	-	nS
td(off)	Turn-Off Delay Time		-	15	-	nS
t_f	Turn-Off Fall Time		-	15	-	nS
Q_g	Total Gate Charge	V_{DS}=100V,I_D=2A, V_{GS}=10V	-	12		nC
Q_{gs}	Gate-Source Charge		-	2.5	-	nC
Q_{gd}	Gate-Drain Charge		-	3.8	-	nC
VSD	Diode Forward Voltage (Note 3)	V_{GS}=0V,I_S=2A	-	-	1.2	V
I_S	Diode Forward Current (Note 2)		-	-	2	A

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

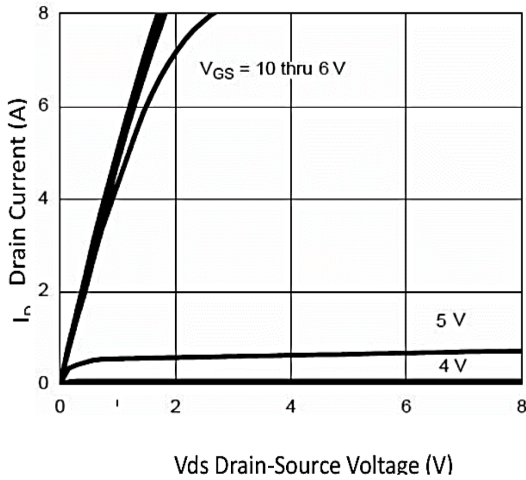


Figure1：Output Characteristics

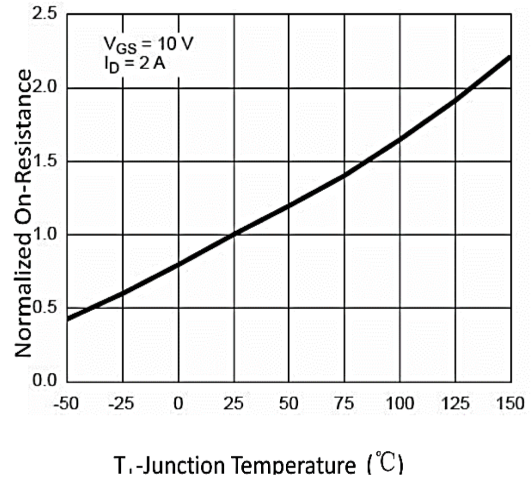


Figure4：Rdson-JunctionTemperature

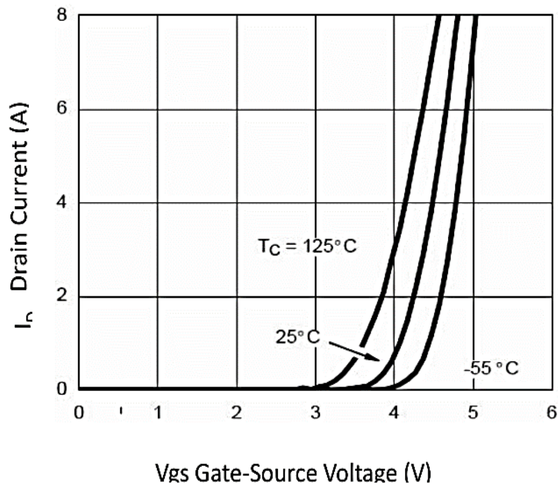


Figure 3：Transfer Characteristics

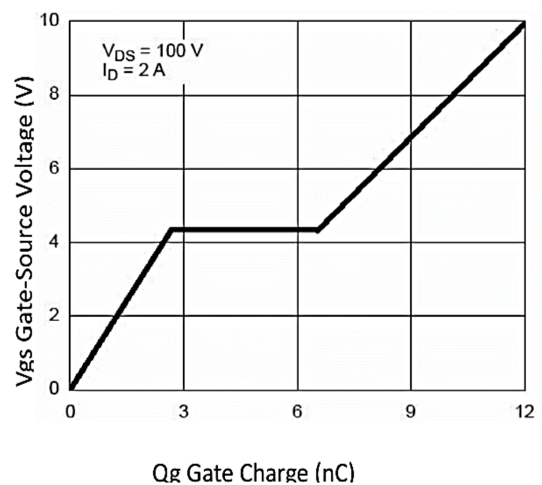


Figure4：Gate Charge

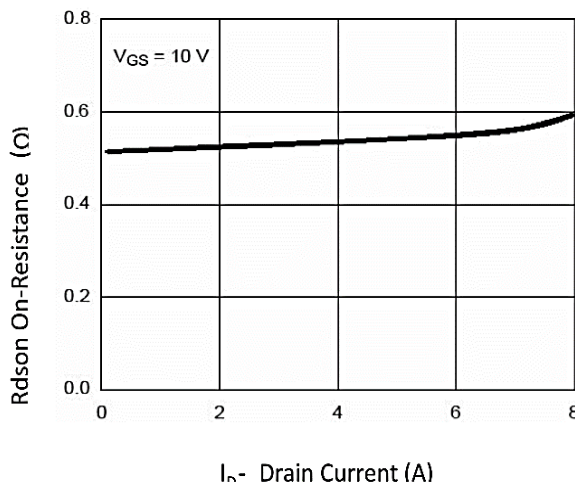


Figure5：Rdson-Drain Current

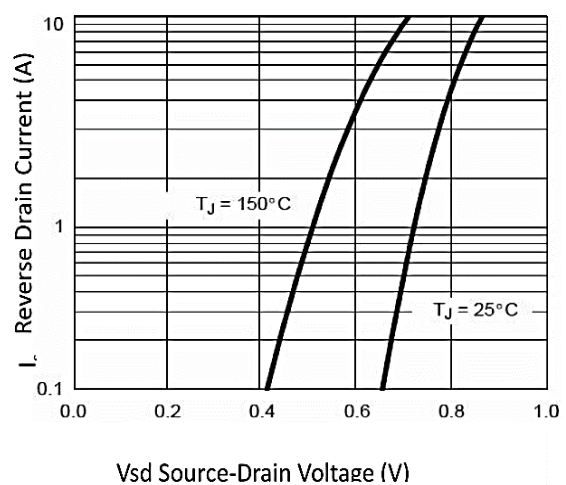


Figure6：Source- Drain Diode Forward

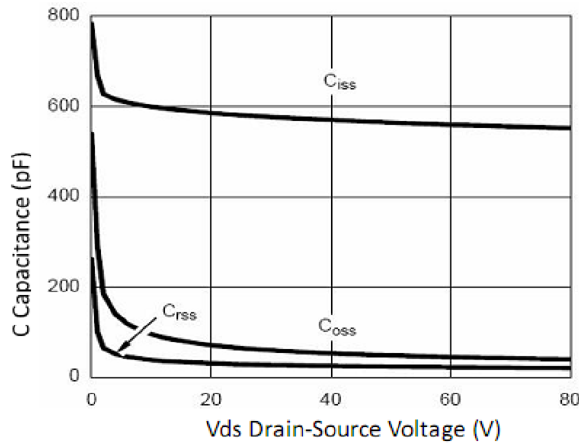


Figure7：Capacitance vs Vds

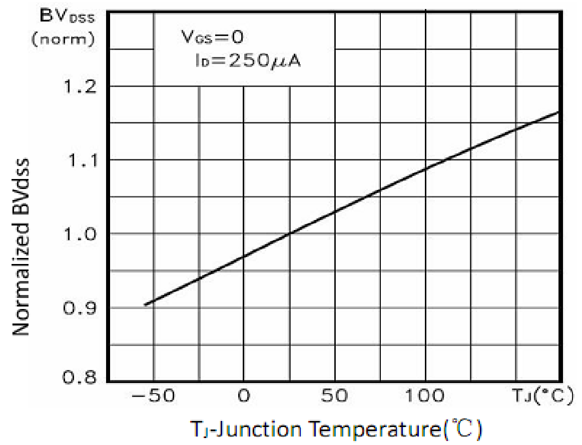


Figure9：BVDSS vs Junction Temperature

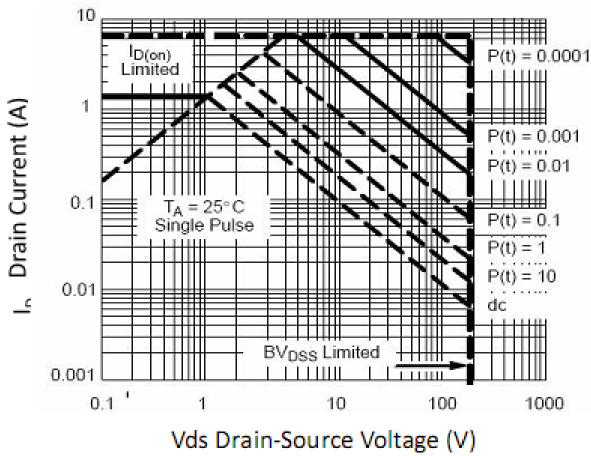


Figure 8：Safe Operation Area

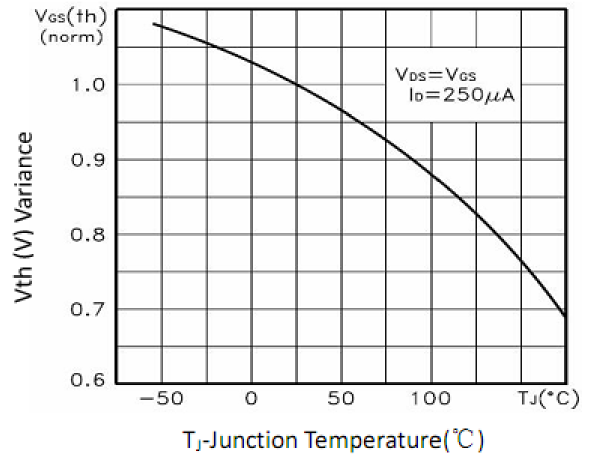


Figure10：VGS(th) vs Junction Temperature

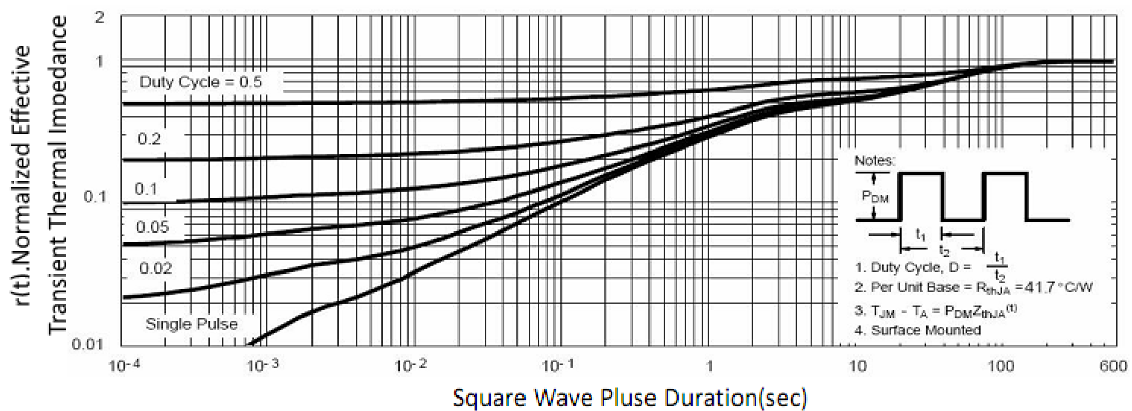
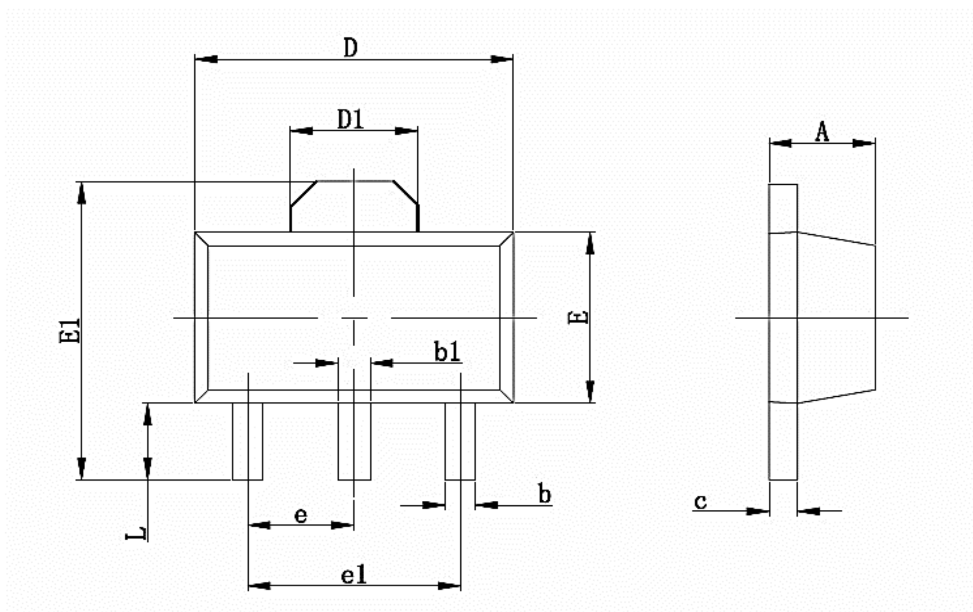


Figure11：Normalized Maximum Transient Thermal Impedance

Package Mechanical Data:SOT89-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.350	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.350	2.550	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060TYP	
e1	3.000 TYP		0.118TYP	
L	0.900	1.100	0.035	0.047