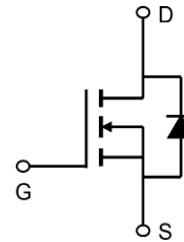


Description

The AP40N15F/P/T uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 150V$ $I_D = 40A$

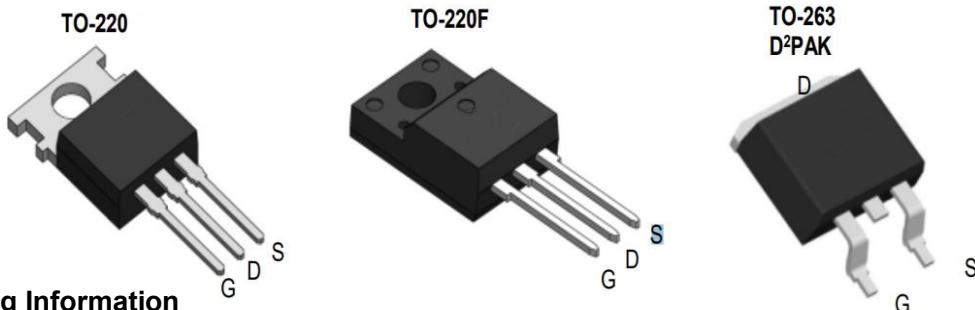
$R_{DS(ON)} < 46m\Omega$ @ $V_{GS}=10V$ (Type: 35m Ω)

Application

DC/DC Converter

LED Backlighting

Power Management Switches



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40N15F	TO-220F-3L	AP40N15F XXX YYYY	1000
AP40N15P	TO-220-3L	AP40N15P XXX YYYY	1000
AP40N15T	TO-263-3L	AP40N15T XXX YYYY	800

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	40	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	28	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	216	mJ
IAS	Avalanche Current	38	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ³	115	W
TSTG	Storage Temperature Range	-55 to 175	°C
T_J	Operating Junction Temperature Range	-55 to 175	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	62.5	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.3	°C/W



150V N-Channel Enhancement Mode MOSFET
Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	150	---	---	V
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	---	35	46	$\text{m}\Omega$
	Static Drain-Source On-Resistance ²	$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$	---	37	50	$\text{m}\Omega$
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.2	2.0	2.5	V
IDSS	Drain-Source Leakage Current	$V_{DS}=120\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=120\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$	---	55	---	S
Q _g	Total Gate Charge (4.5V)	$V_{DS}=75\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=10\text{A}$	---	40	---	nC
Qgs	Gate-Source Charge		---	10	---	
Qgd	Gate-Drain Charge		---	21	---	
Td(on)	Turn-On Delay Time	$V_{DD}=50\text{V}$, $V_{GS}=4.5\text{V}$, $R_G=3.3\Omega$, $I_D=10\text{A}$	---	18	---	ns
T _r	Rise Time		---	20	---	
Td(off)	Turn-Off Delay Time		---	65	---	
T _f	Fall Time		---	15	---	
C _{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	3755	---	pF
C _{oss}	Output Capacitance		---	207	---	
C _{rss}	Reverse Transfer Capacitance		---	160	---	
I _S	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	30	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
trr	Reverse Recovery Time	IF=10A, $dI/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	35	---	nS
Q _{rr}	Reverse Recovery Charge		---	120	---	nC

Notes:

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $L=0.5\text{mH}$, $I_{AS}=38\text{A}$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

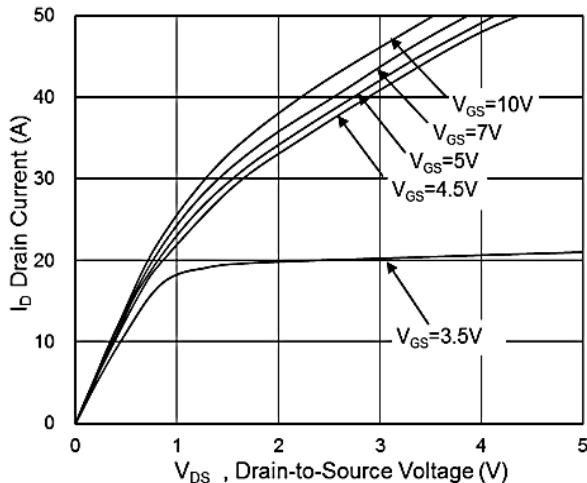


Fig.1 Typical Output Characteristics

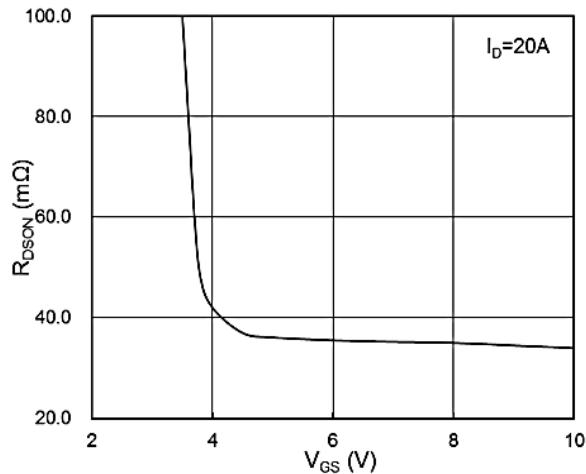


Fig.2 On-Resistance vs. Gate-Source

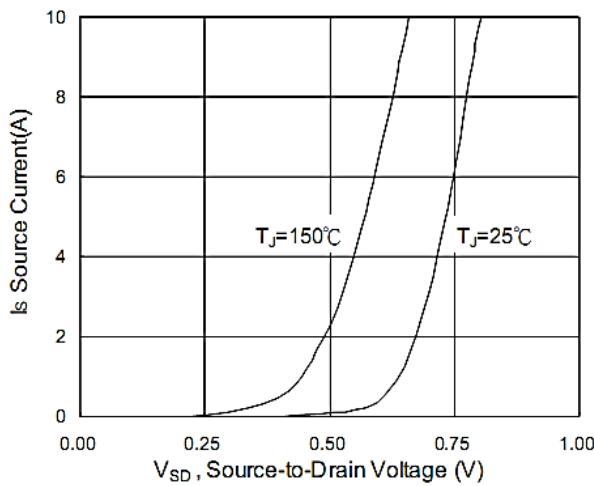


Fig.3 Forward Characteristics Of Reverse

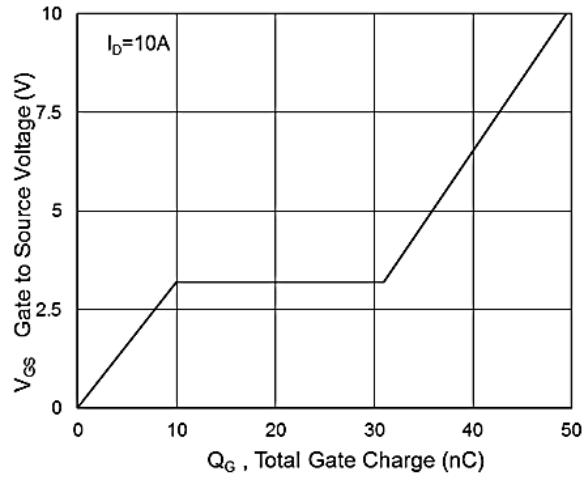


Fig.4 Gate-Charge Characteristics

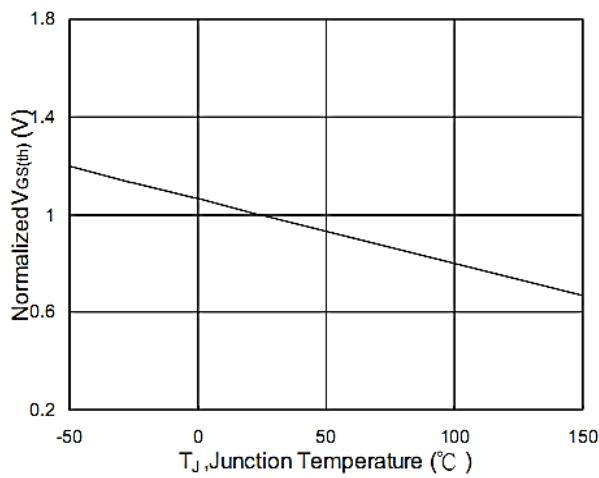


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

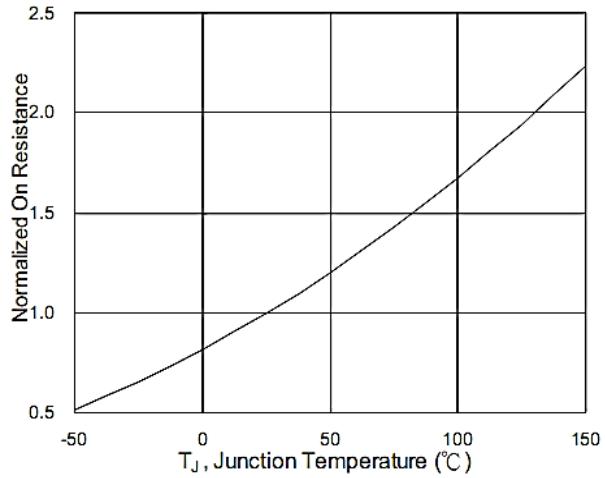


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

150V N-Channel Enhancement Mode MOSFET

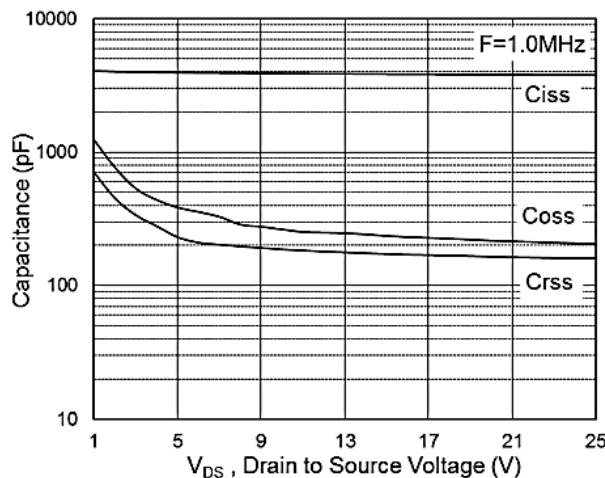


Fig.7 Capacitance

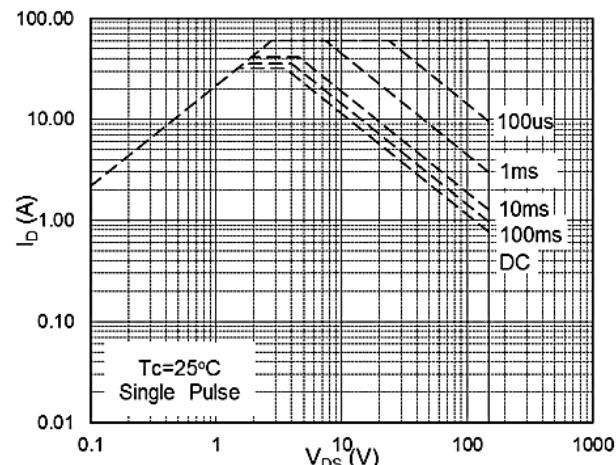


Fig.8 Safe Operating Area

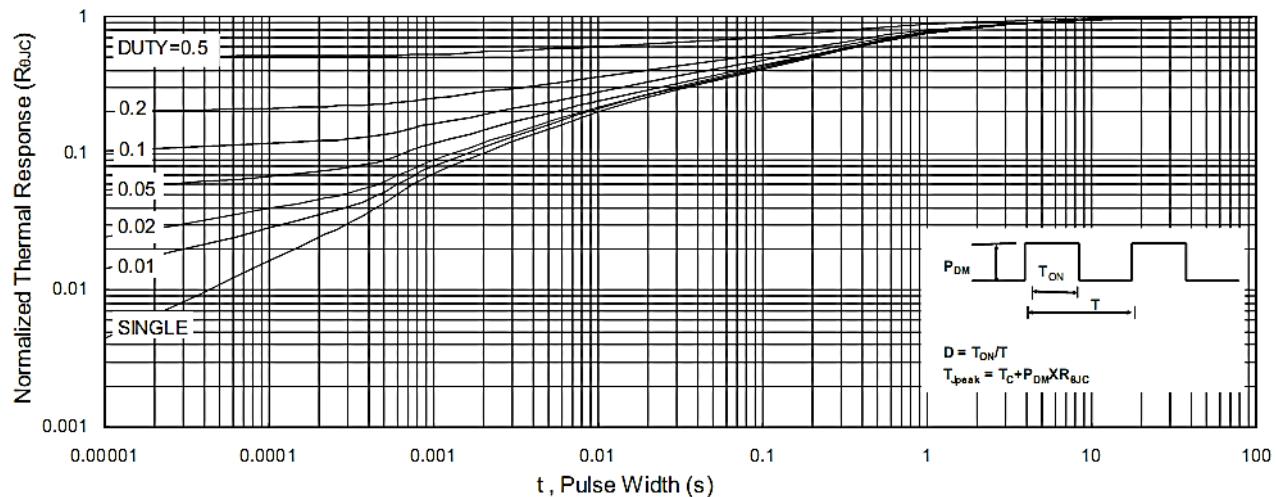


Fig.9 Normalized Maximum Transient Thermal Impedance

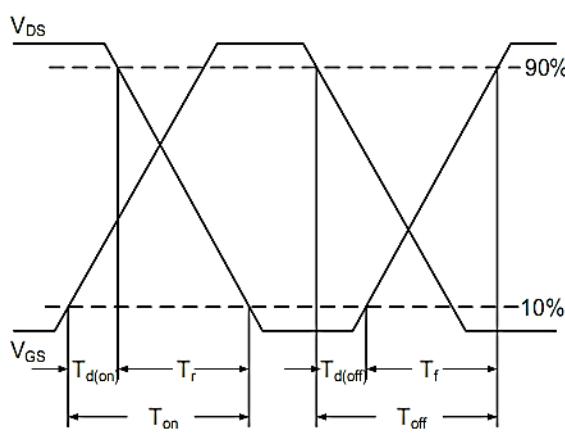


Fig.10 Switching Time Waveform

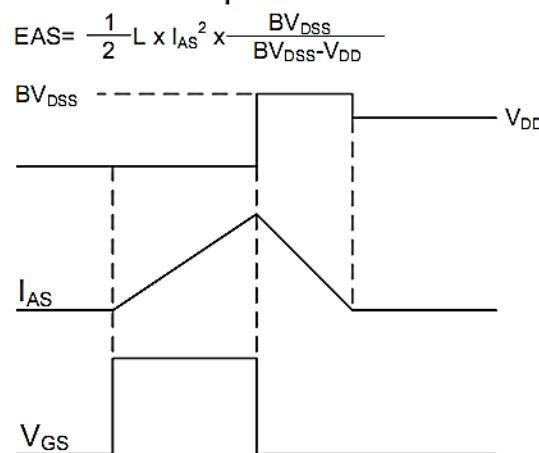
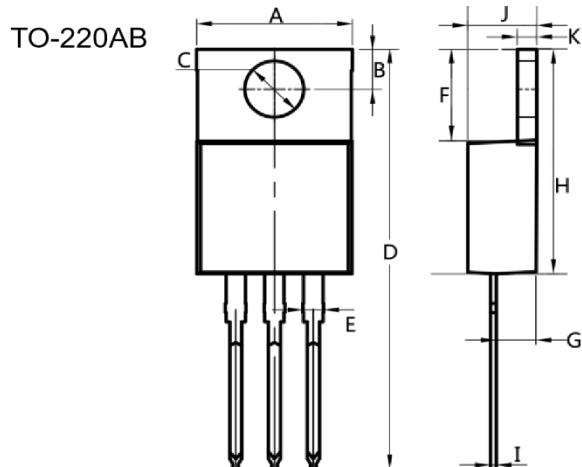
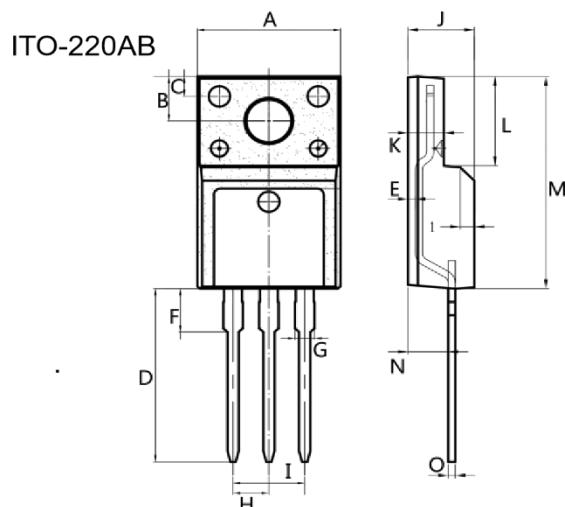


Fig.11 Unclamped Inductive Switching Waveform



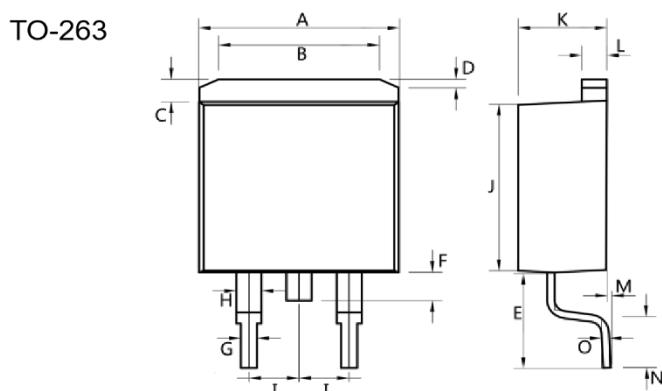
Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4

All Dimensions in millimeter



Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60

All Dimensions in millimeter



Dim.	Min.	Max.
A	10.0	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45

All Dimensions in millimeter