AP18N15S

150V N-Channel Enhancement Mode MOSFET

Description

The AP18N15S uses advanced **SGT II** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 150V I_D =28A

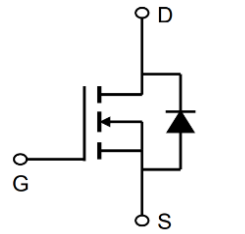
$R_{DS(ON)}$ < 78mΩ@ V_{GS}=10V **（Type：63mΩ）**

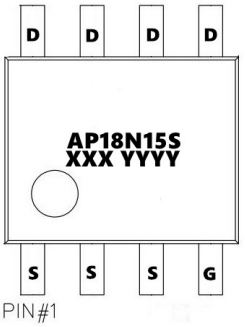
Application

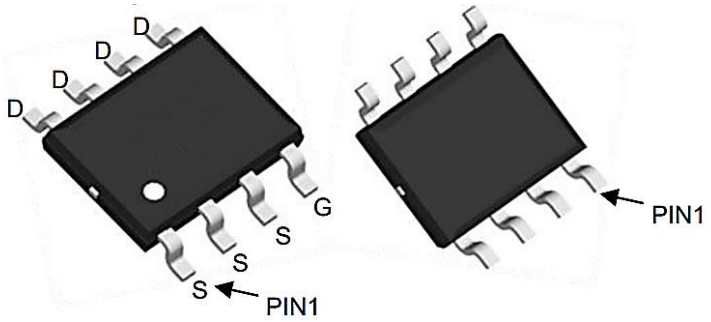
Automative lighting

Load switch

Uninterruptible power supply







Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP18N15S	SOP-8L	AP18N15S XXX YYYY	3000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	150	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	18	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	11	A
IDM	Pulsed Drain Current[1]	54	A
P_D@T_C=25℃	Total Power Dissipation	60	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Maximum Thermal Resistance, Junctionambient	85	℃/W
RθJC	Maximum Thermal Resistance, Junction-case	2.5	℃/W

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150V N-Channel Enhancement Mode MOSFET

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	150	175	-	V
IGSS	Gate-body Leakage current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T_J= 25℃	V_{DS} = 150V, V_{GS} = 0V	-	-	1	
IDSS	Zero Gate Voltage Drain Current T_J= 100℃		-	-	100	
VGS(th)	Gate-Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.8	3.0	V
RDS(on)	Drain-Source On-Resistance[2]	V_{GS} = 10V, I_D = 10A	-	63	78	mΩ
RDS(on)	Drain-Source On-Resistance[2]	V_{GS} = 4.5V, I_D = 8A		72	90	
gfs	Transconductance	V_{DS}= 5V, I_D= 10A	-	23	-	S
Ciss	Input Capacitance	V_{DS} = 75V, V_{GS} = 0V, f = 1MHz	-	630	-	pF
Coss	Output Capacitance		-	50	-	
Crss	Reverse Transfer Capacitance		-	13.5	-	
R_g	Gate Resistance	V_{GS} = 0V, V_{DS} Open, f = 1MHz	-	5	-	Ω
Q_g	Total Gate Charge	V_{GS} = 10V,V_{DD} = 75V, I_D= 10A	-	11	-	nC
Qgs	Gate-Source Charge		-	1.2	-	
Qgd	Gate-Drain Charge		-	4	-	
td(on)	Turn-On Delay Time	V_{GS} = 10V, V_{DD} = 75V, R_G = 10Ω, I_D= 10A	-	9.8	-	nS
t_r	Rise Time		-	6	-	
td(off)	Turn-Off Delay Time		-	15	-	
t_f	Fall Time		-	4.1	-	
VSD	Diode Forward Voltage[2]	I_S = 10A, V_{GS} = 0V	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	V_R = 75V,I_F = 10A, dI/dt= 100A/μs	-	55	-	nS
Q_{rr}	Body Diode Reverse Recovery Charge		-	124	-	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

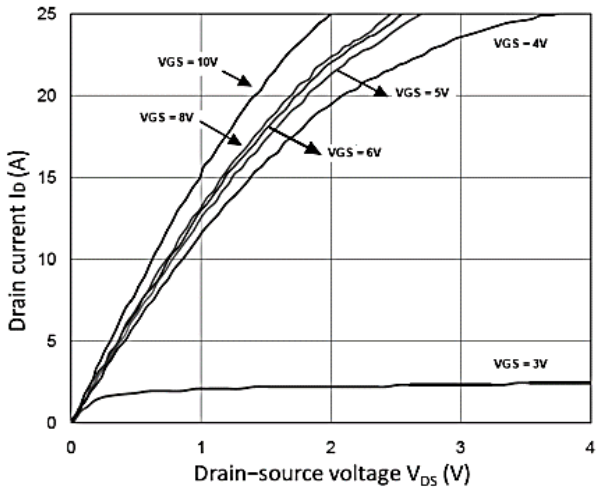


Figure 1. Output Characteristics

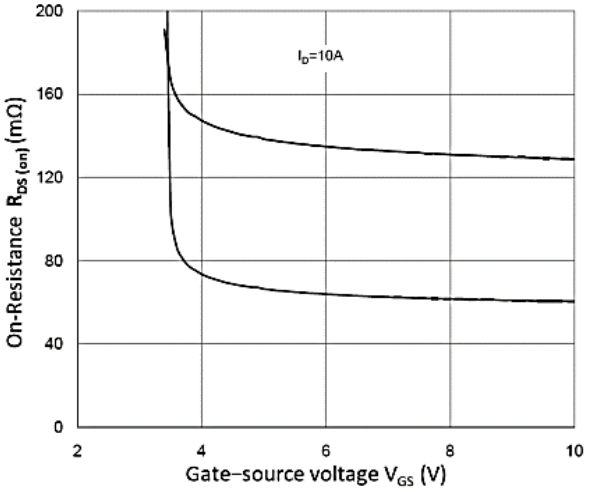


Figure 2. R DS (on) vs. V GS

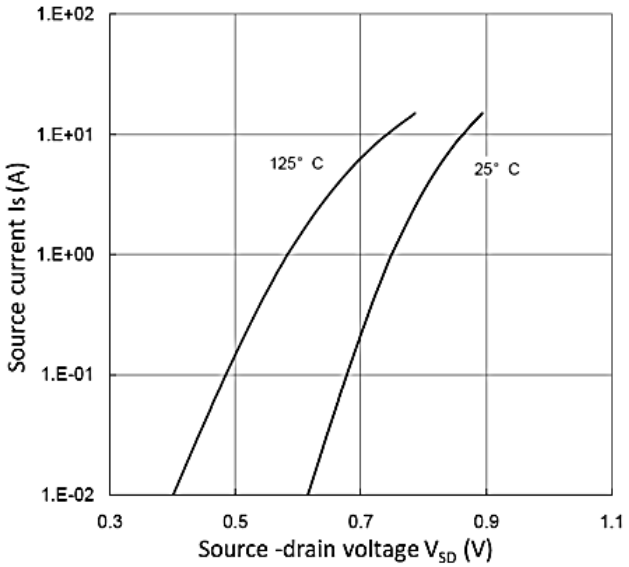


Figure 3. Forward Characteristics of Reverse

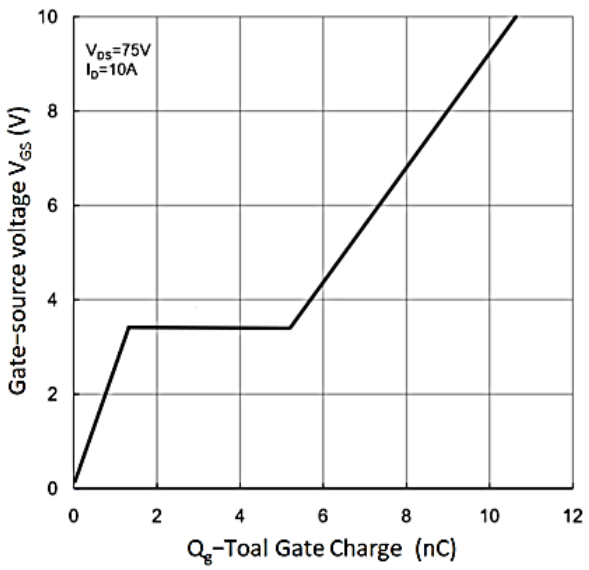


Figure 4. Gate Charge Characteristics

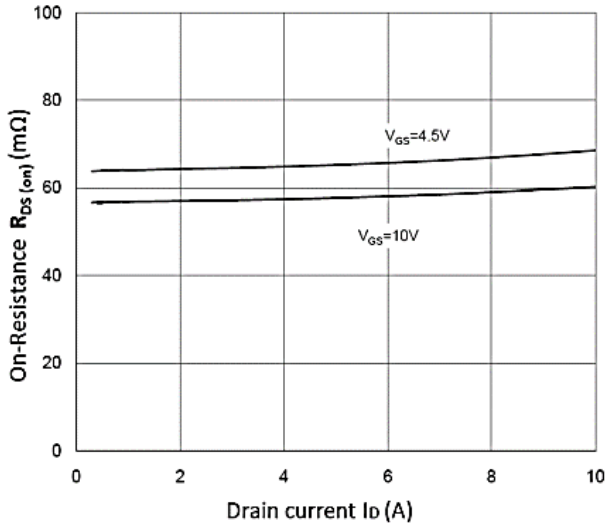


Figure 5. RDS(ON) vs. ID

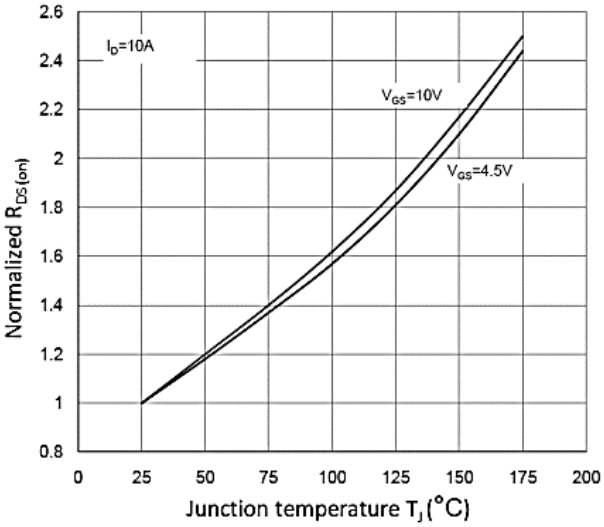


Figure 6. Normalized RDS(on) vs. TJ

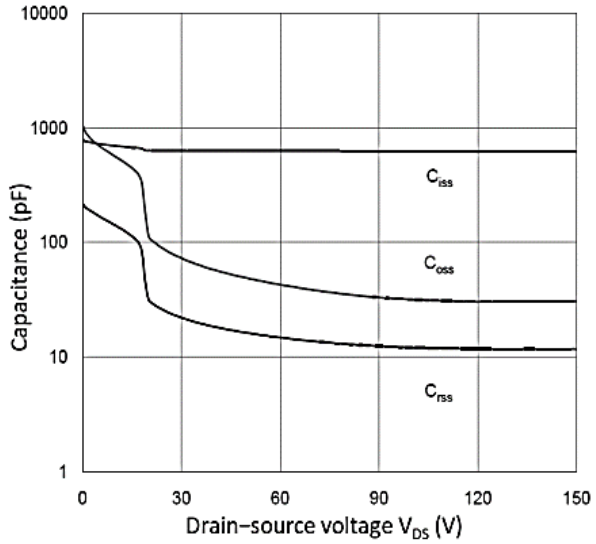


Figure 7. Capacitance Characteristics

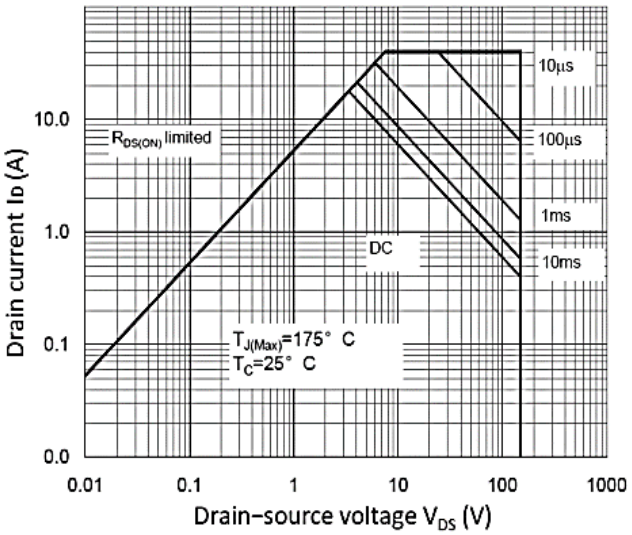


Figure 8. Safe Operating Area

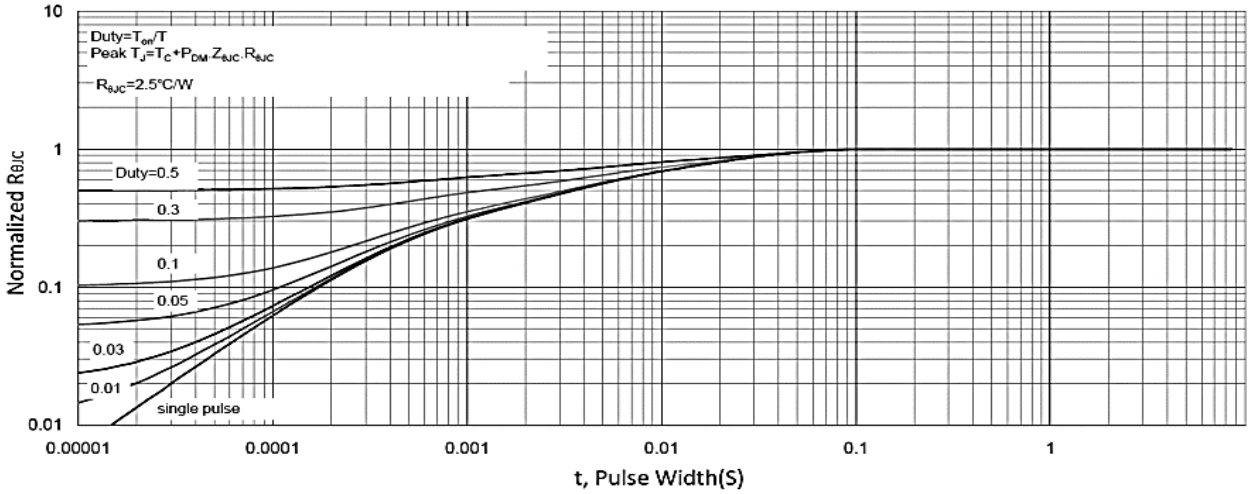


Figure 9. Normalized Maximum Transient Thermal Impedance

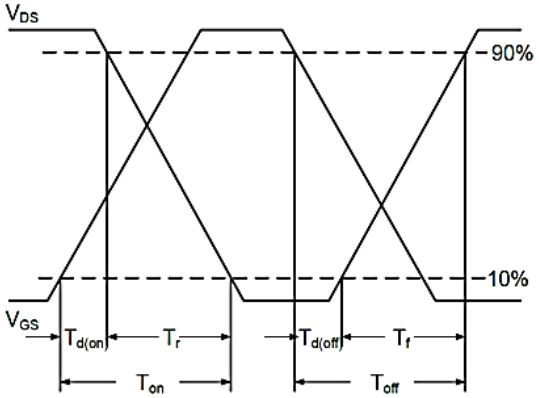


Figure 10. Switching Time Waveform

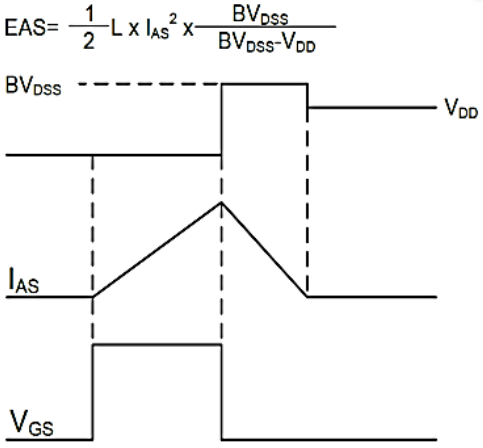
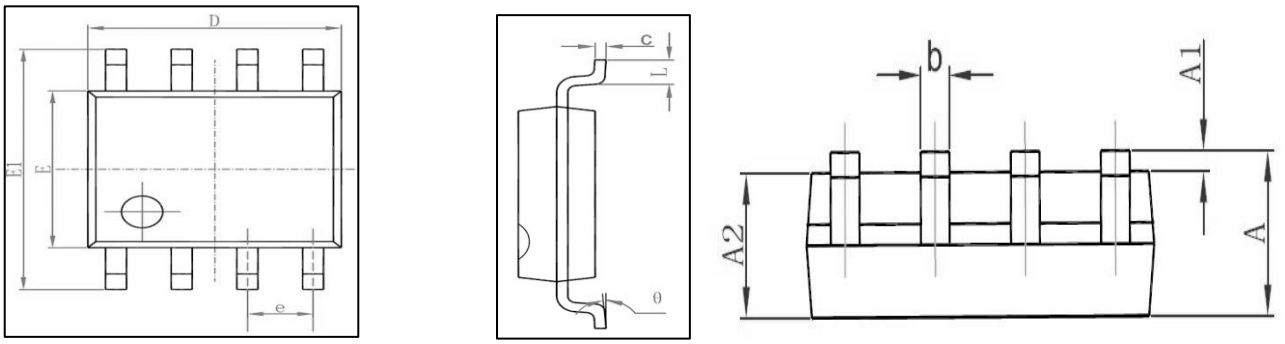
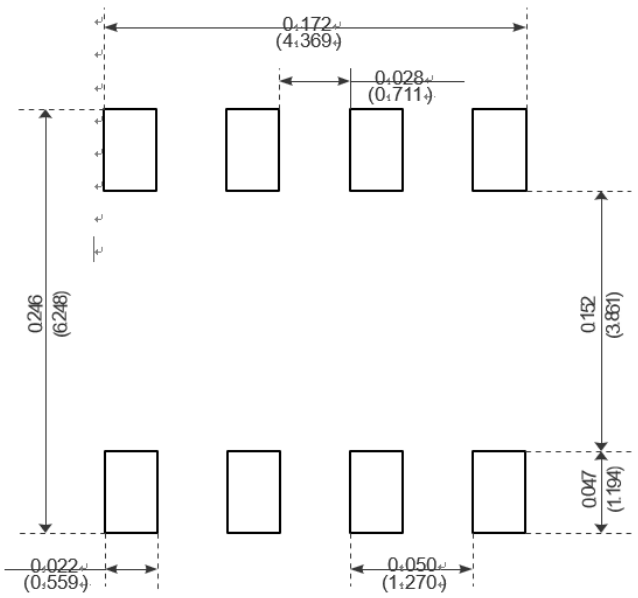


Figure 11. Unclamped Inductive Switching

Package Mechanical Data-SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads