

## 120V N-Channel Enhancement Mode MOSFET

### Description

The AP50N12D uses advanced **SGT II** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 120V$   $I_D = 50A$

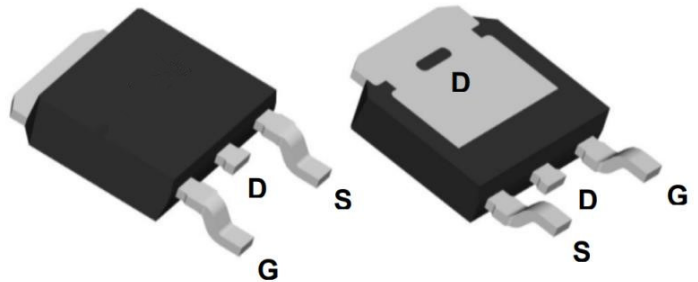
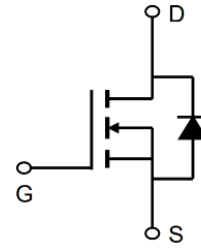
$R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=10V$  (**Type: 25mΩ**)

### Application

Mobile phone fast charging

Brushless motor

Home appliance control board



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50N12D	TO-252-3L	AP50N12D XXX YYYY	2500

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	120	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current <sup>1</sup>	48	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current <sup>1</sup>	34	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	150	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	6	mJ
$I_{AS}$	Avalanche Current	5	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>3</sup>	113	W
$T_{STG} T_J$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	62.5	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.1	$^\circ\text{C/W}$



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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

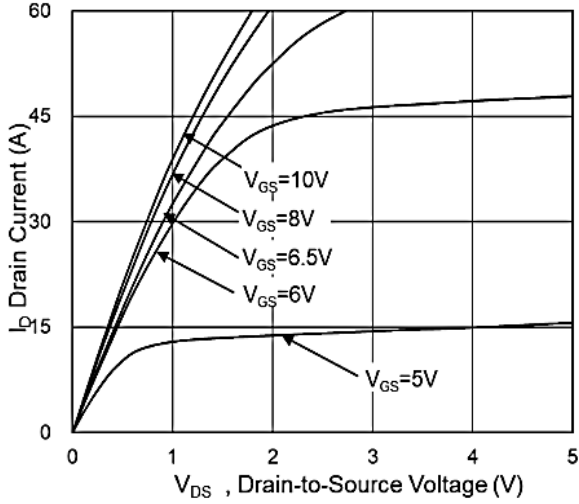
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	120	135	---	V
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	25	32	mΩ
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	2.0	3.0	4.0	V
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =96V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =96V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	---	50	---	S
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	20.6	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	6.9	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	5.1	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =1A	---	12.7	---	ns
T <sub>r</sub>	Rise Time		---	8.2	---	
Td(off)	Turn-Off Delay Time		---	30.3	---	
T <sub>f</sub>	Fall Time		---	13.3	---	
Ciss	Input Capacitance	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHz	---	1362	---	pF
Coss	Output Capacitance		---	192	---	
Crss	Reverse Transfer Capacitance		---	3.7	---	
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	20	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =10A, T <sub>J</sub> =25°C	---	---	1.2	V
trr	Reverse Recovery Time	IF=20A, dI/dt=100A/μs, T <sub>J</sub> =25°C	---	55	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	163	---	nC

#### Note :

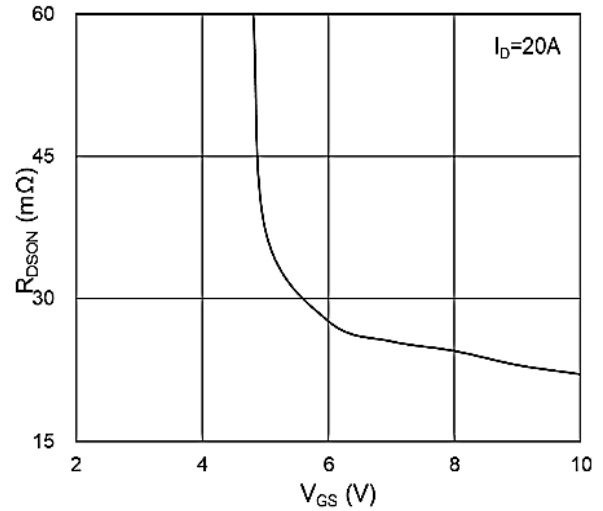
- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 20Z copper.
- 2、 The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、 The power dissipation is limited by 175°C junction temperature
- 4、 EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>= 50V, V<sub>G</sub>= 10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>= 30A
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

**120V N-Channel Enhancement Mode MOSFET**

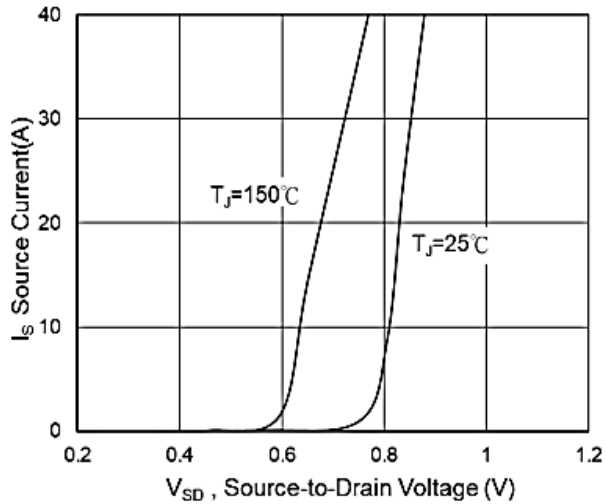
**Typical Characteristics**



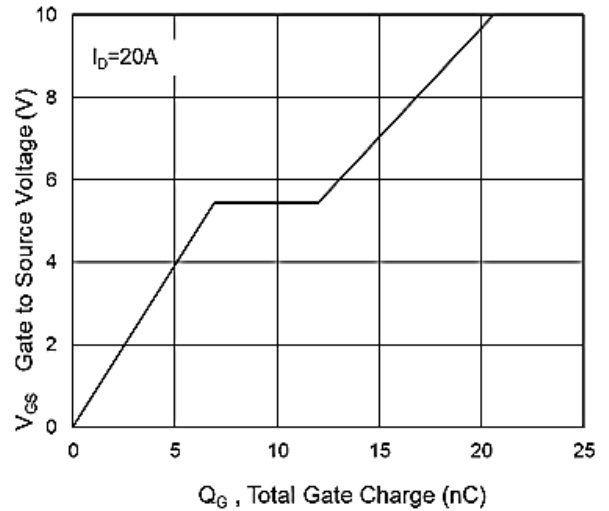
**Fig.1 Typical Output Characteristics**



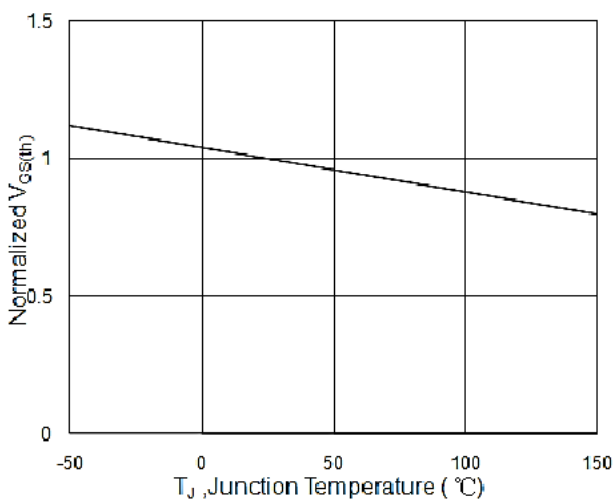
**Fig.2 On-Resistance vs G-S Voltage**



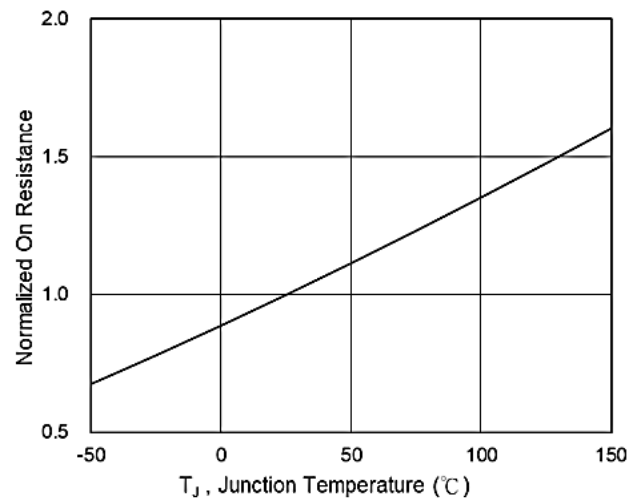
**Fig.3 Source Drain Forward Characteristics**



**Fig.4 Gate-Charge Characteristics**

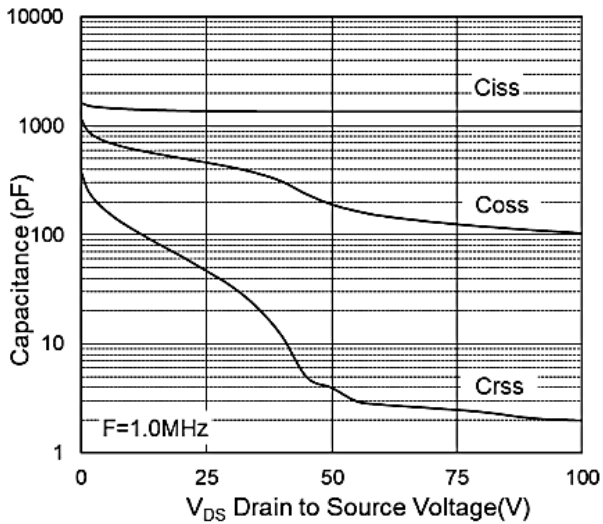


**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**

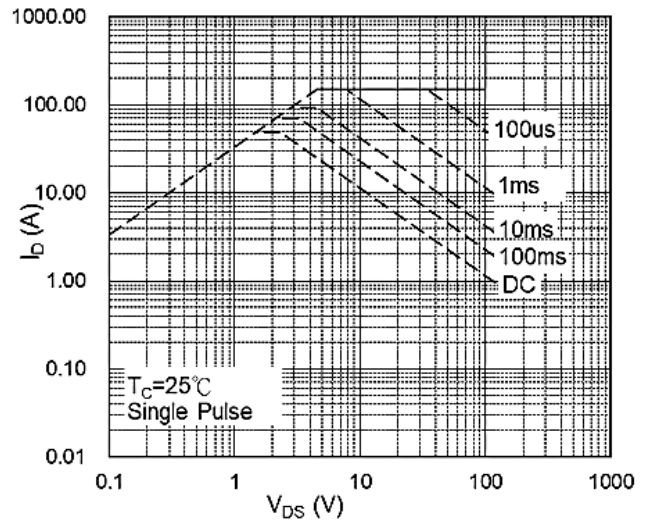


**Fig.6 Normalized  $R_{DSON}$  vs  $T_J$**

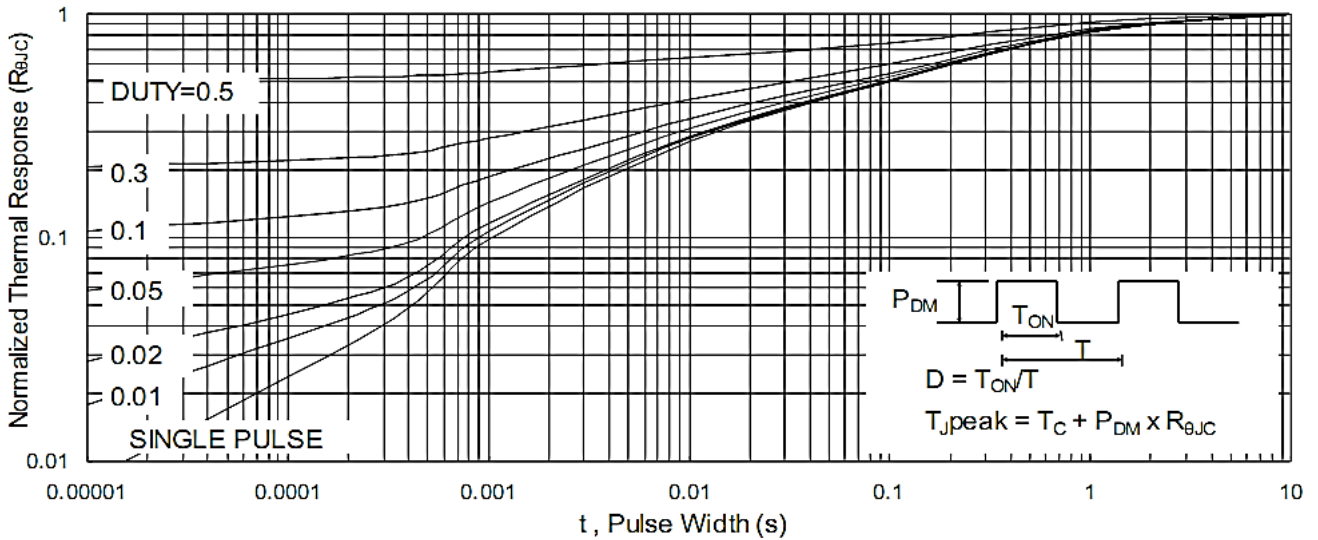
**120V N-Channel Enhancement Mode MOSFET**



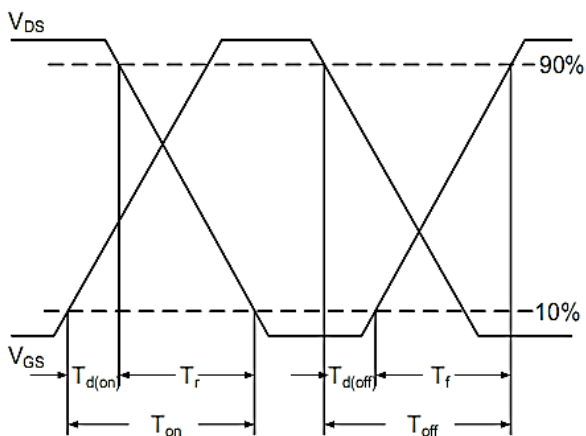
**Fig.7 Capacitance**



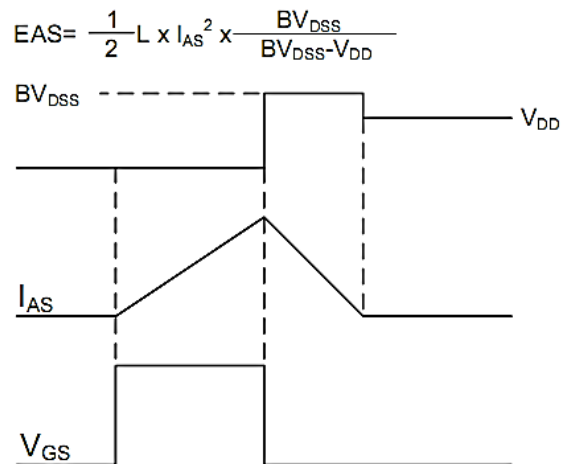
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



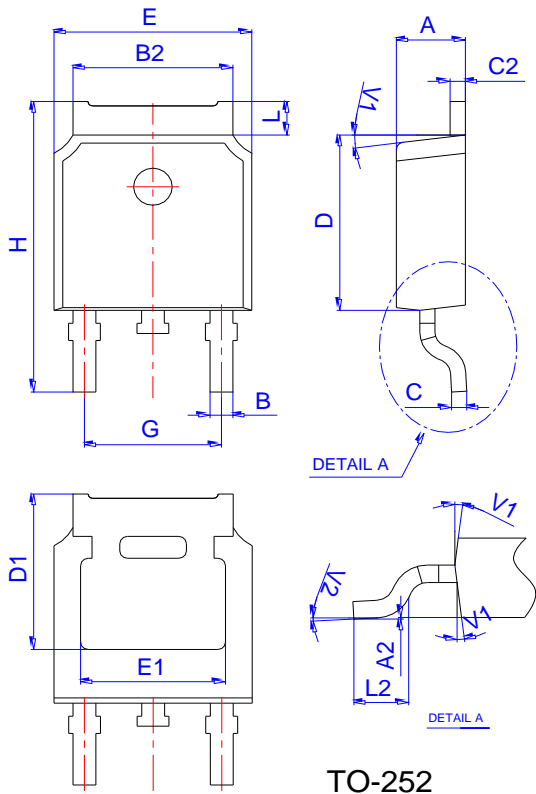
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

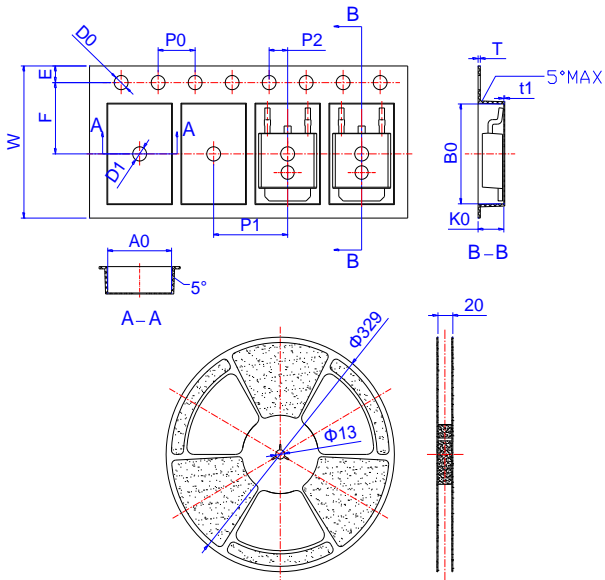
$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

### Package Mechanical Data:TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2		0°	6°		0°	6°

### Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583