

## 100V N-Channel Enhancement Mode MOSFET

### Description

The AP200N10MP uses advanced SGT<sub>1.1</sub> technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 200A$

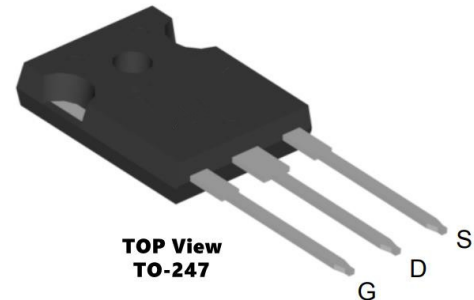
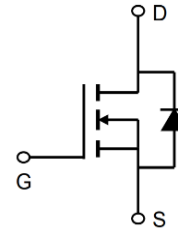
$R_{DS(ON)} < 5.0m\Omega$  @  $V_{GS}=10V$  (Type: 4.1m $\Omega$ )

### Application

DC/DC Converter

LED Backlighting

Power Management Switches



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP200N10MP	TO-247-3L	AP200N10MP XXX YYYY	300

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V	200	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V	125	A
IDM	Pulsed Drain Current	580	A
EAS	Single Pulse Avalanche Energy	540	mJ
IAS	Avalanche Current	53.4	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	148	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	0.42	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case	40	$^\circ C/W$

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### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

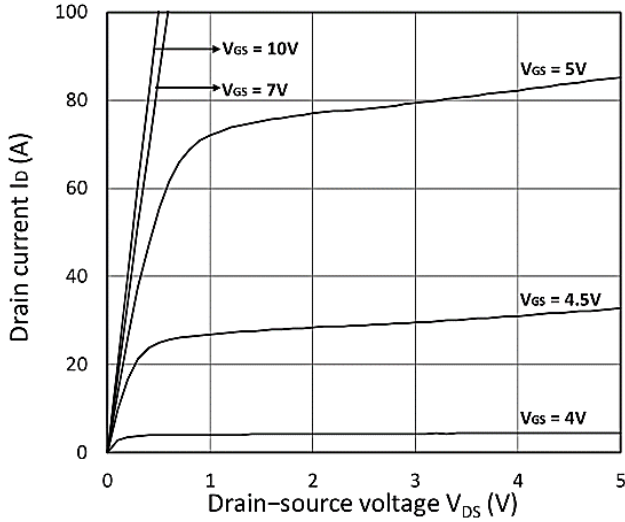
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100	107	-	V
IGSS	Gate-body Leakage current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T <sub>J</sub> =25°C	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	-	-	1	μA
	Zero Gate Voltage Drain Current T <sub>J</sub> =100°C		-	-	100	
VGS(th)	Gate-Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source on-Resistance <sup>4</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	4.1	5.0	mΩ
gfs	Forward Transconductance <sup>4</sup>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A	-	62	-	S
Ciss	Input Capacitance	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V, f = 1MHz	-	6865	-	pF
Coss	Output Capacitance		-	740	-	
Crss	Reverse Transfer Capacitance		-	21	-	
R <sub>g</sub>	Gate Resistance	f = 1MHz	-	1.3	-	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 50V, I <sub>D</sub> = 20A	-	111.2	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	30.5	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	27.3	-	
td(on)	Turn-on Delay Time	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 50V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	33	-	ns
t <sub>r</sub>	Rise Time		-	39	-	
td(off)	Turn-off Delay Time		-	67.1	-	
t <sub>f</sub>	Fall Time		-	32	-	
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = 20A, dI/dt = 100A/μs	-	58.7	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	97.3	-	nC
VSD	Diode Forward Voltage <sup>4</sup>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V
IS	Continuous Source Current T <sub>C</sub> =25°C	-	-	-	120	A

#### Notes:

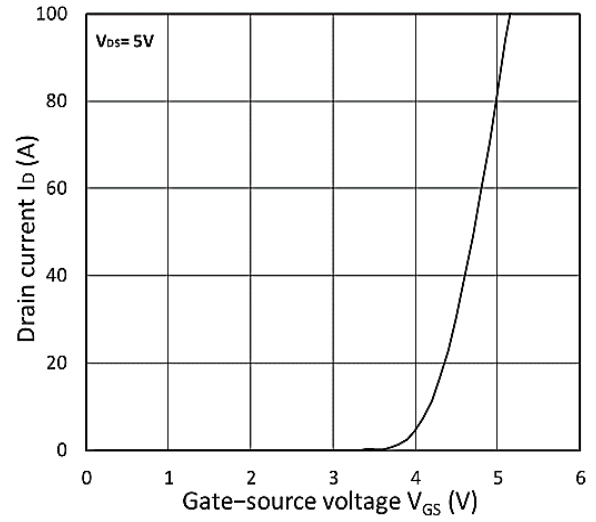
- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.4mH, I<sub>AS</sub>=32A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

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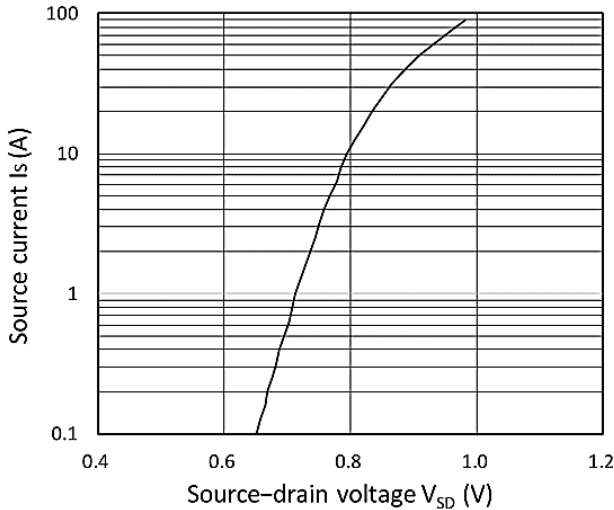
**Typical Characteristics**



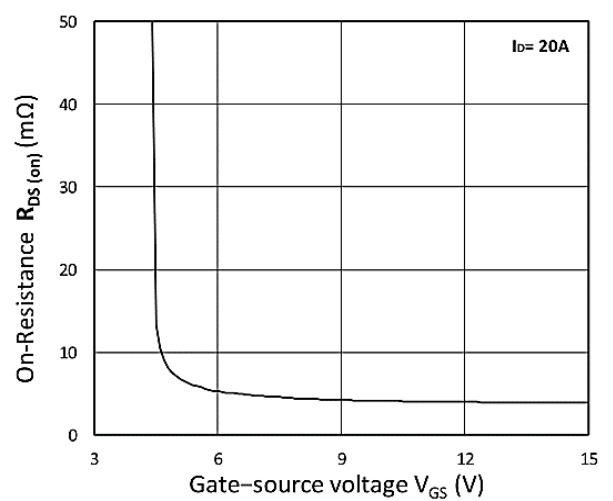
**Figure 1. Output Characteristics**



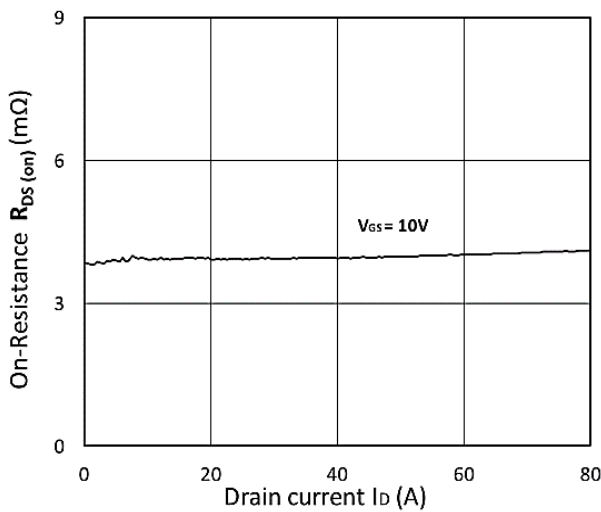
**Figure 2. Transfer Characteristics**



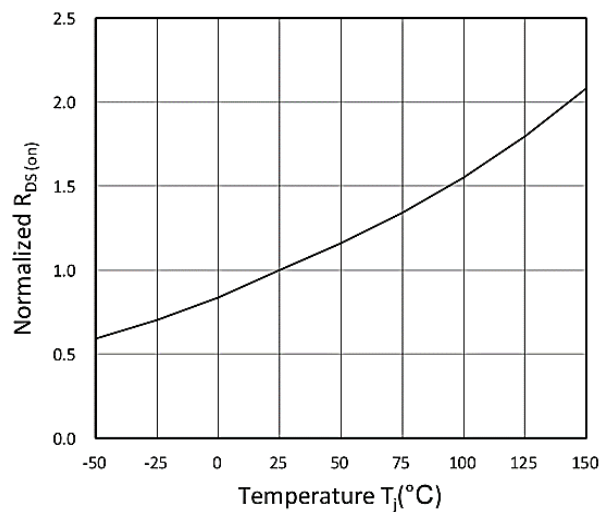
**Figure 3. Forward Characteristics of Reverse**



**Figure 4. RDS(ON) vs. VGS**



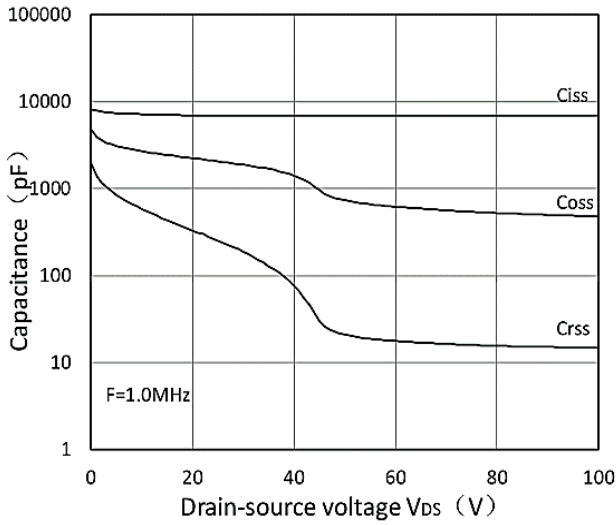
**Figure 5. RDS(ON) vs. ID**



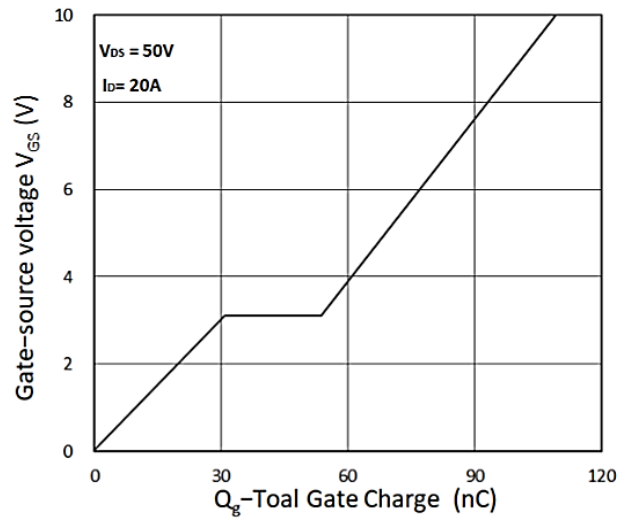
**Figure 6. Normalized RDS(on) vs. Temperature**



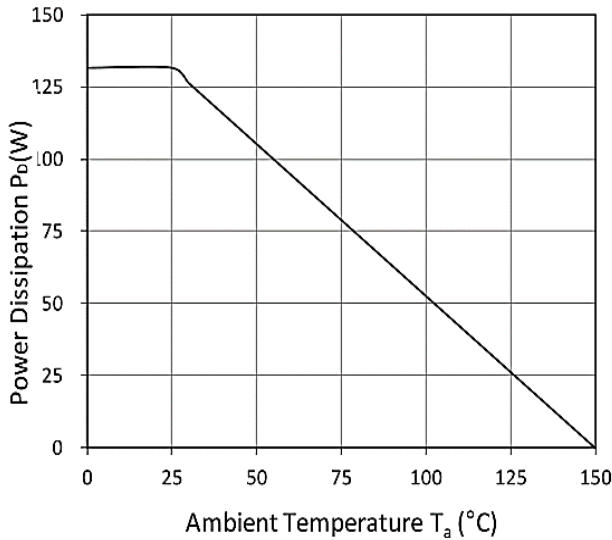
**100V N-Channel Enhancement Mode MOSFET**



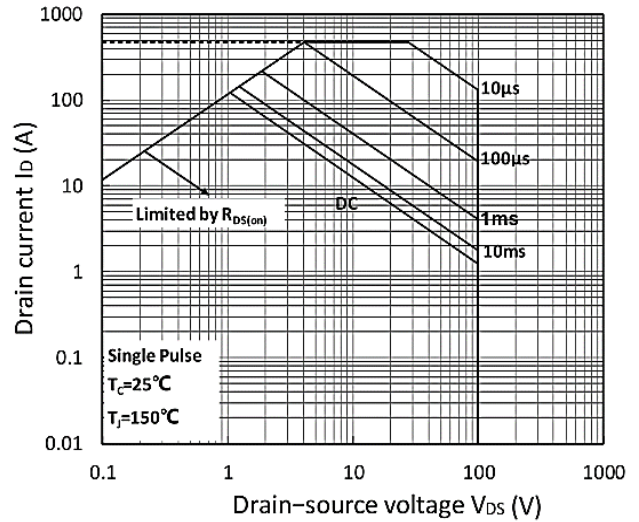
**Figure 7. Capacitance Characteristics**



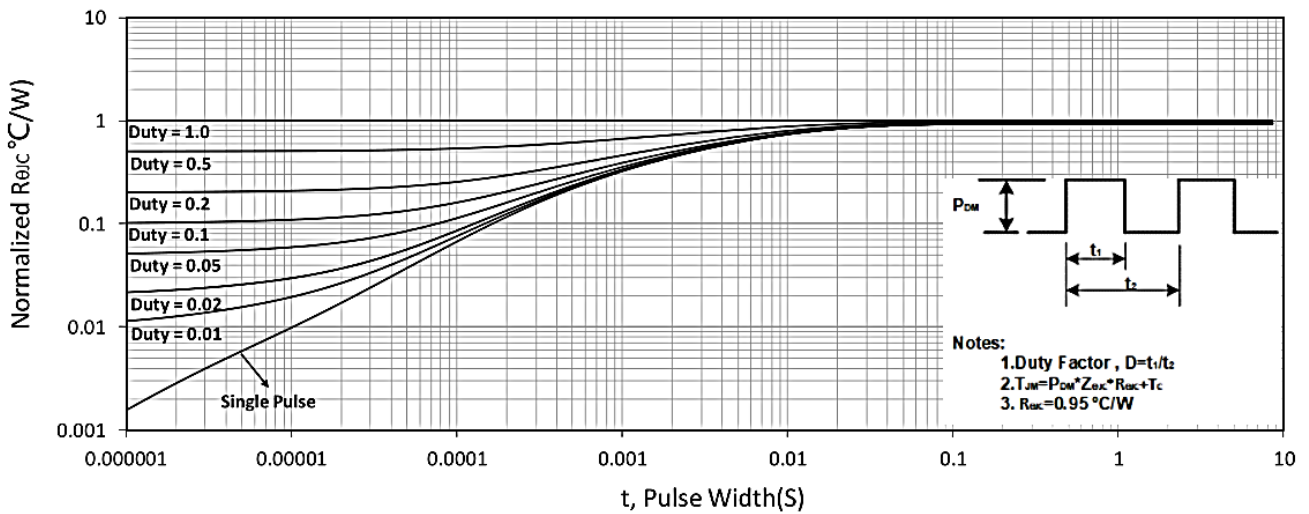
**Figure 8. Gate Charge Characteristics**



**Figure 9. Power Dissipation**



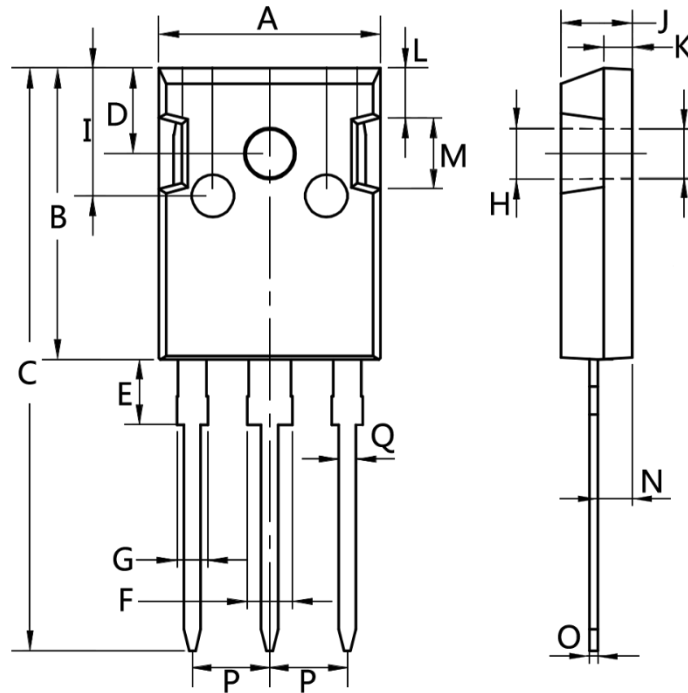
**Figure 10. Safe Operating Area**



**Figure 11. Normalized Maximum Transient Thermal Impedance**

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### Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3