

100V N-Channel Enhancement Mode MOSFET

Description

The AP5N10DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 100V$ $I_D = 5A$

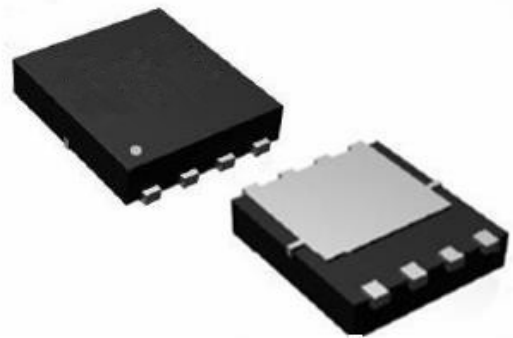
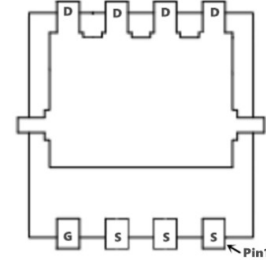
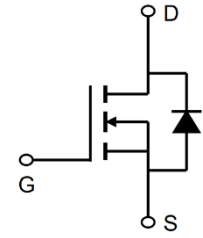
$R_{DS(ON)} < 140m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N10DF	PDFN3*3-8L	AP5N10DF	5000

Absolute Maximum Ratings at $T_j=25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ C$	I_D	5	A
Pulsed drain current ²⁾ , $T_C=25^\circ C$	$I_{D, pulse}$	15	A
Power dissipation ³⁾ , $T_C=25^\circ C$	P_D	17	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	1.2	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ C$
Thermal resistance, junction-case	$R_{\theta JC}$	7.4	$^\circ C/W$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^\circ C/W$



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Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source breakdown voltage	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	100			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	1.2	2.0	2.5	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS}=10\text{ V}, I_D=5\text{ A}$		110	140	m Ω
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS}=4.5\text{ V}, I_D=3\text{ A}$		160	180	m Ω
I_{GSS}	Gate-source leakage current	$V_{GS}=20\text{ V}$			100	nA
		$V_{GS}=-20\text{ V}$			-100	
I_{DSS}	Drain-source leakage current	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}$			1	μA
C_{iss}	Input capacitance	$V_{GS}=0\text{ V},$ $V_{DS}=50\text{ V},$ $f=100\text{ kHz}$		206.1		pF
C_{oss}	Output capacitance			28.9		pF
C_{rss}	Reverse transfer capacitance			1.4		pF
$t_{d(on)}$	Turn-on delay time			14.7		ns
t_r	Rise time	$V_{GS}=10\text{ V},$ $V_{DS}=50\text{ V},$ $R_G=2\text{ }\Omega,$ $I_D=5\text{ A}$		3.5		ns
$t_{d(off)}$	Turn-off delay time			20.9		ns
t_f	Fall time			2.7		ns
Q_g	Total gate charge			4.3		nC
Q_{gs}	Gate-source charge	$I_D=5\text{ A},$ $V_{DS}=50\text{ V},$ $V_{GS}=10\text{ V}$		1.5		nC
Q_{gd}	Gate-drain charge			1.1		nC
$V_{plateau}$	Gate plateau voltage			5.0		V
I_S	Diode forward current	$V_{GS}<V_{th}$			7	A
I_{SP}	Pulsed source current				21	
V_{SD}	Diode forward voltage	$I_S=7\text{ A}, V_{GS}=0\text{ V}$			1.0	V
t_{rr}	Reverse recovery time	$I_S=5\text{ A}, di/dt=100$		32.1		ns
Q_{rr}	Reverse recovery charge			39.4		nC
I_{rrm}	Peak reverse recovery current		$\text{A}/\mu\text{s}$		2.1	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.
- 5) $V_{DD}=50\text{ V}, R_G=50\text{ }\Omega, L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

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Electrical Characteristics Diagrams

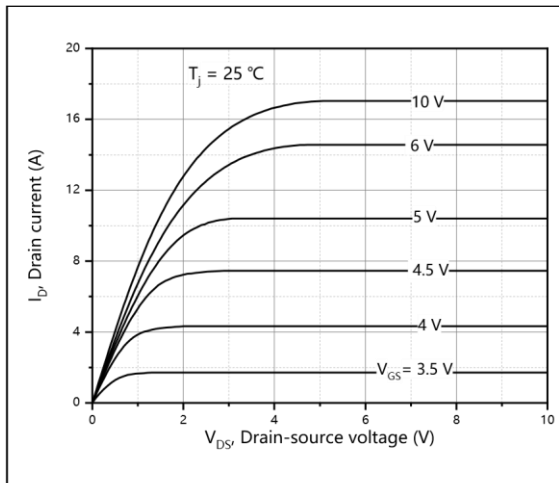


Figure 1, Typ. output characteristics

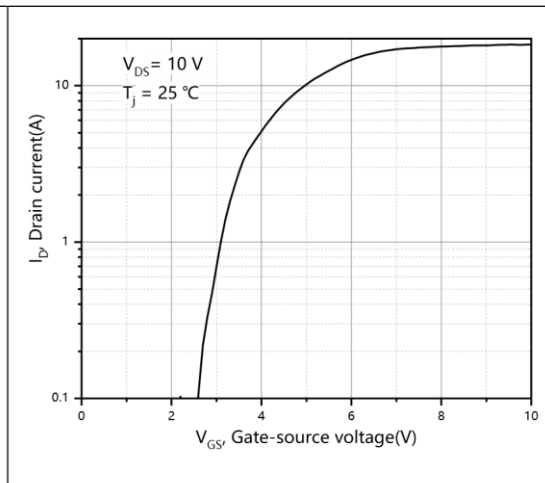


Figure 2, Typ. transfer characteristics

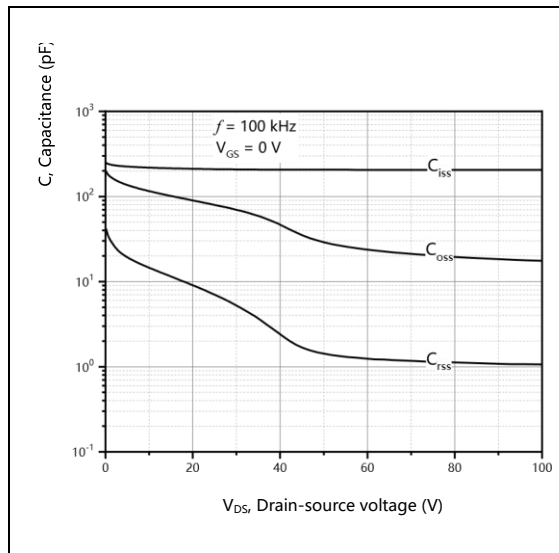


Figure 3, Typ. capacitances

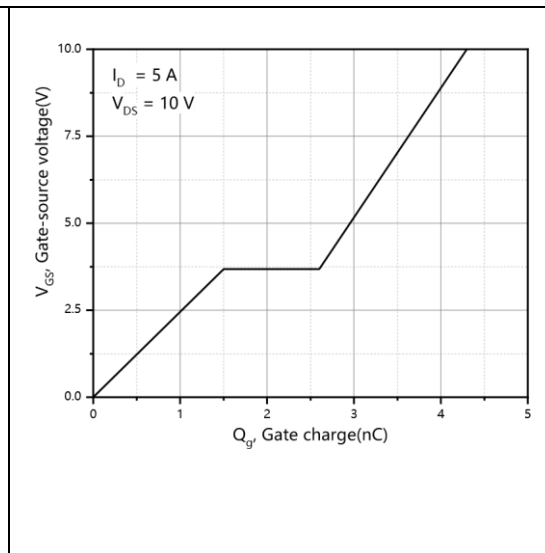


Figure 4, Typ. gate charge

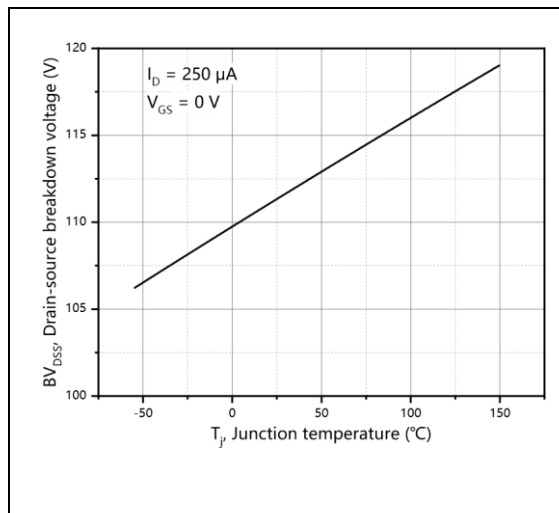


Figure 5, Drain-source breakdown voltage

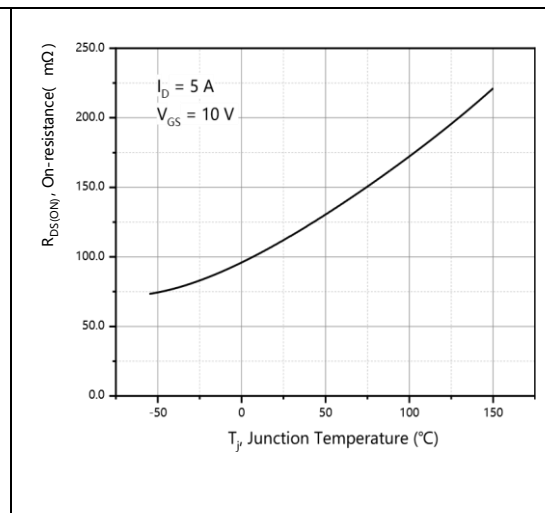


Figure 6, Drain-source on-state resistance

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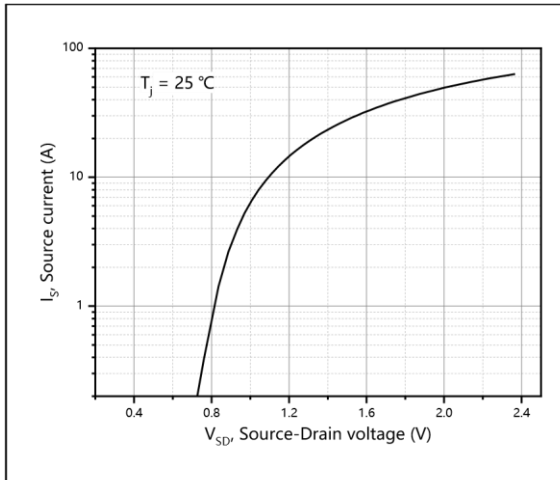


Figure 7, Forward characteristic of body diode

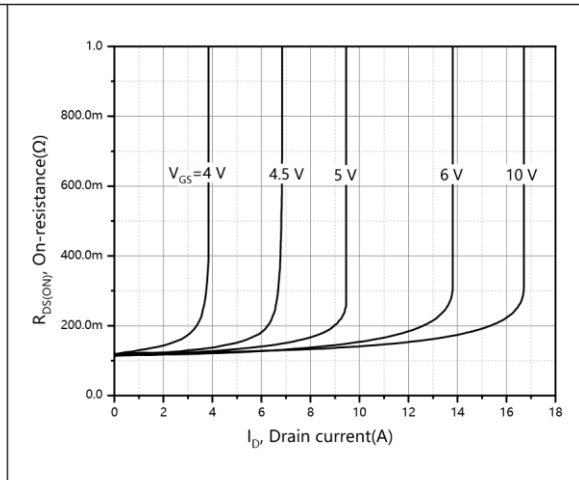


Figure 8, Drain-source on-state resistance

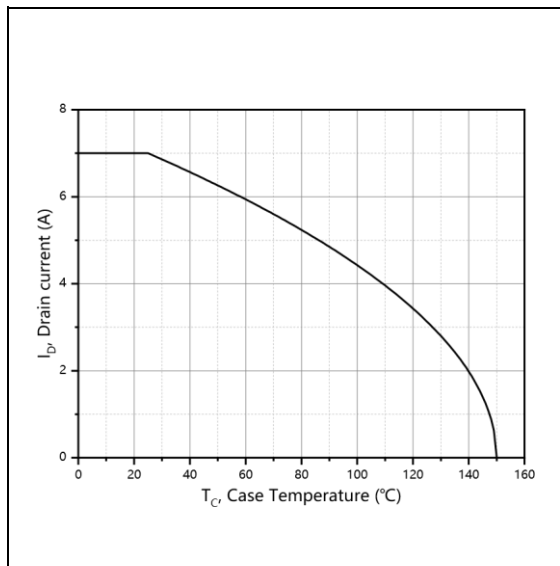


Figure 9, Drain current

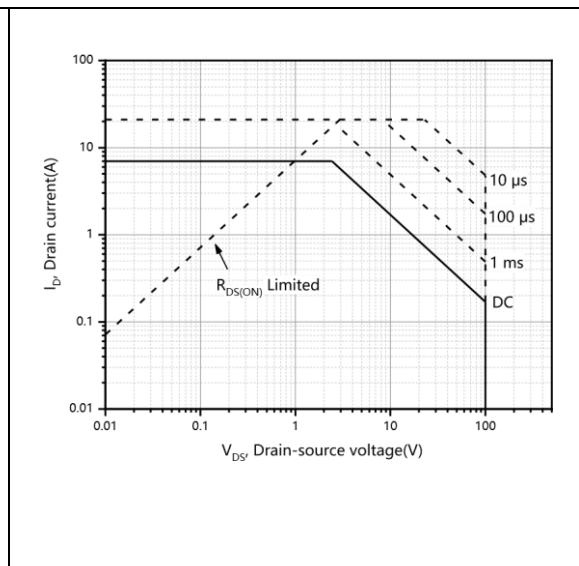


Figure 10, Safe operation area $T_C=25\text{ °C}$

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Test circuits and waveforms

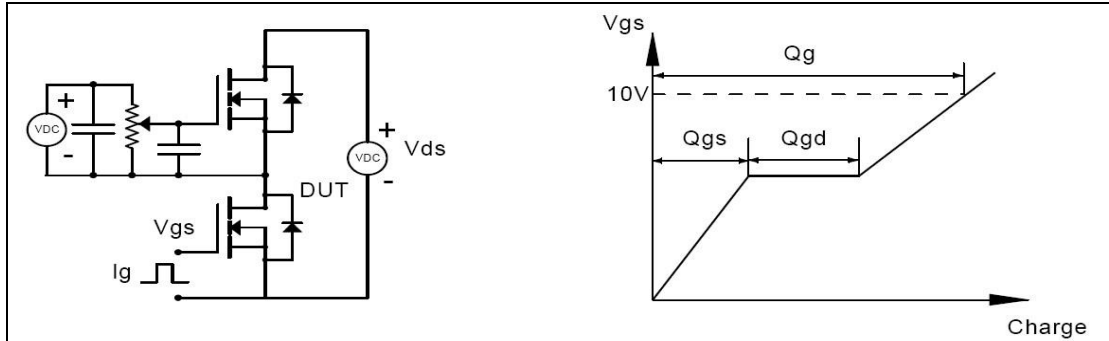


Figure 1, Gate charge test circuit & waveform

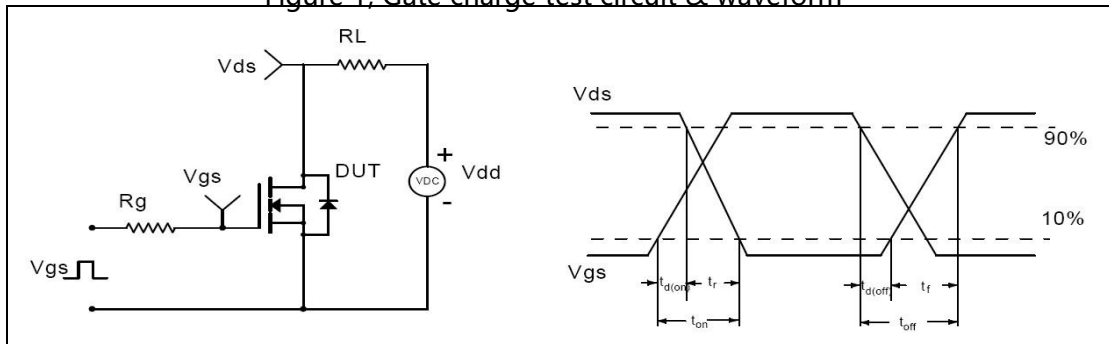


Figure 2, Switching time test circuit & waveforms

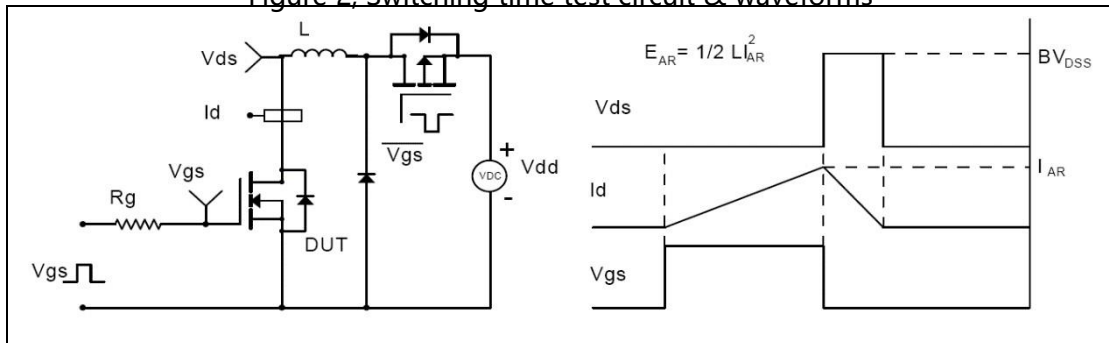


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

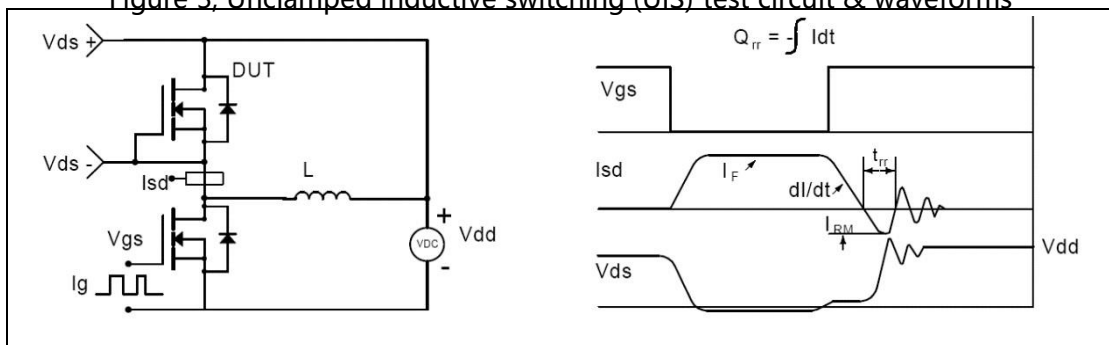
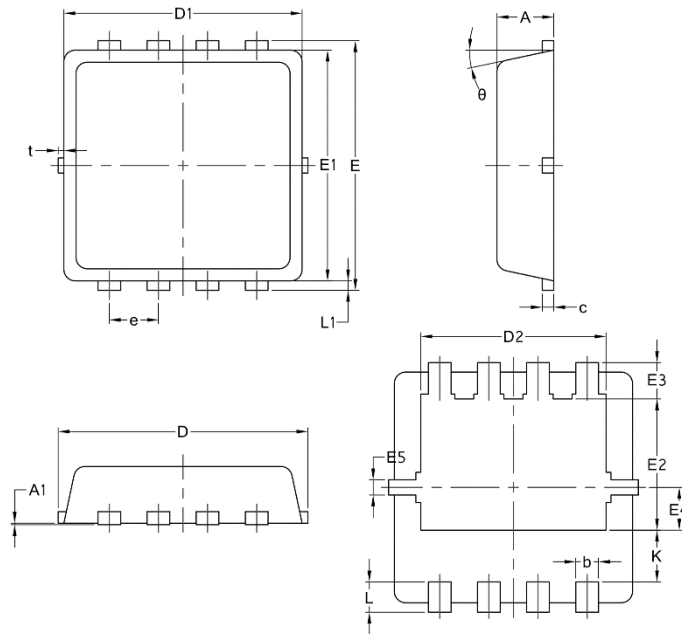


Figure 4, Diode reverse recovery test circuit & waveforms

100V N-Channel Enhancement Mode MOSFET Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14