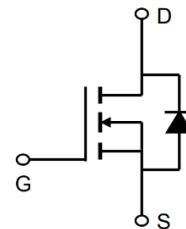


Description

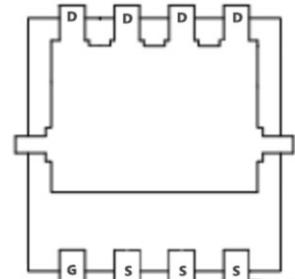
The AP40N06DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 60V$ $I_D = 40A$

$R_{DS(ON)} < 32m\Omega$ @ $V_{GS}=10V$ (Type: 20m Ω)

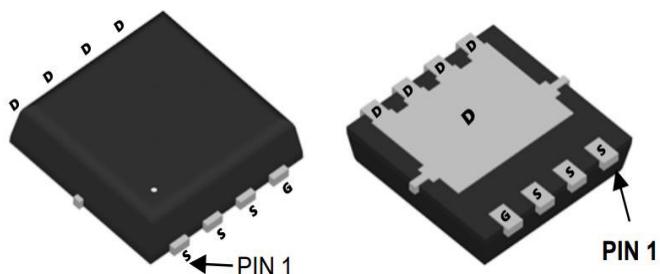


Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40N06DF	PDFN3*3-8L	AP40N06DF XXXXX YYYY	5000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	40	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	18	A
I_{DM}	Pulsed Drain Current ²	114	A
EAS	Single Pulse Avalanche Energy ³	25.5	mJ
I_{AS}	Avalanche Current	22	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ⁴	34.7	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	3.6	°C/W

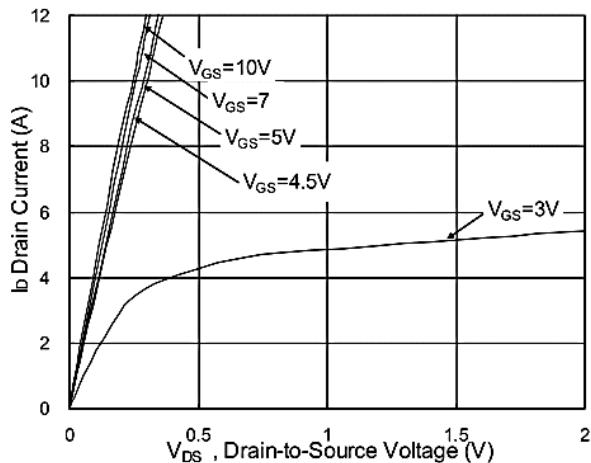
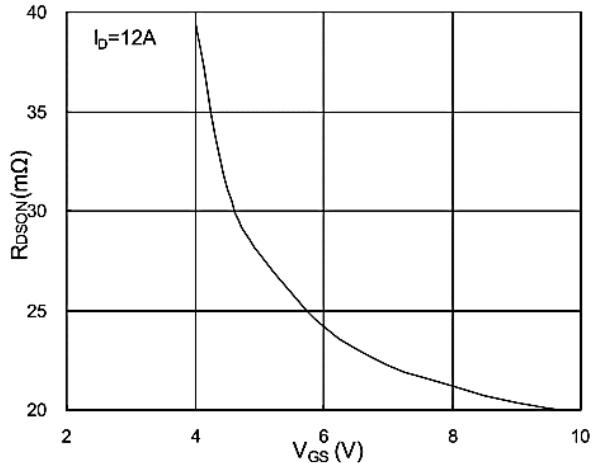
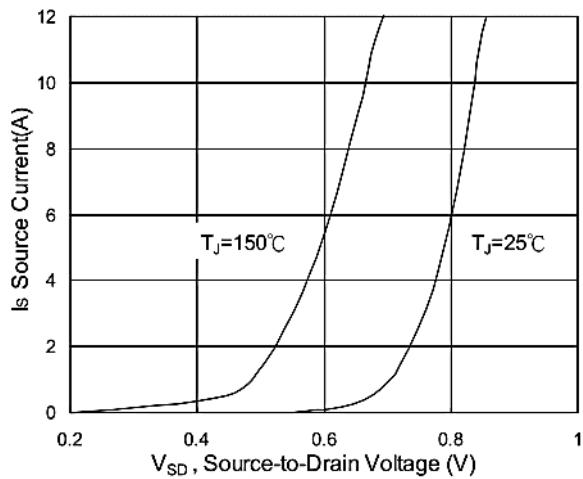
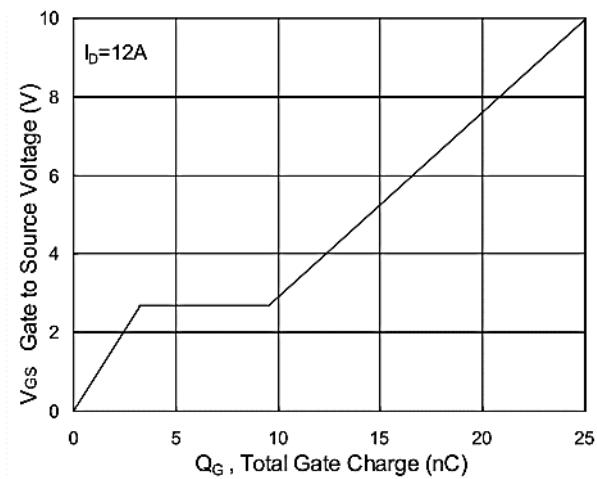
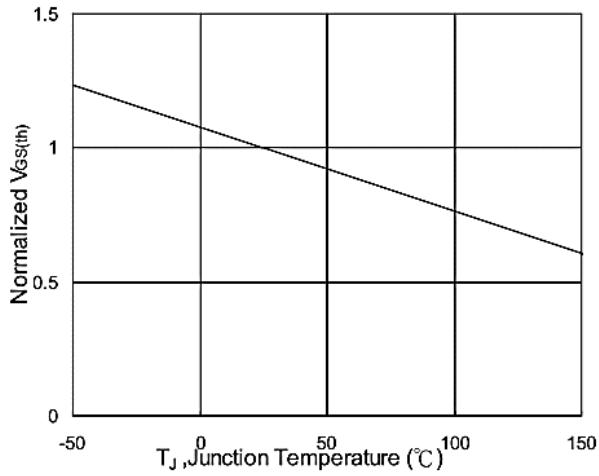
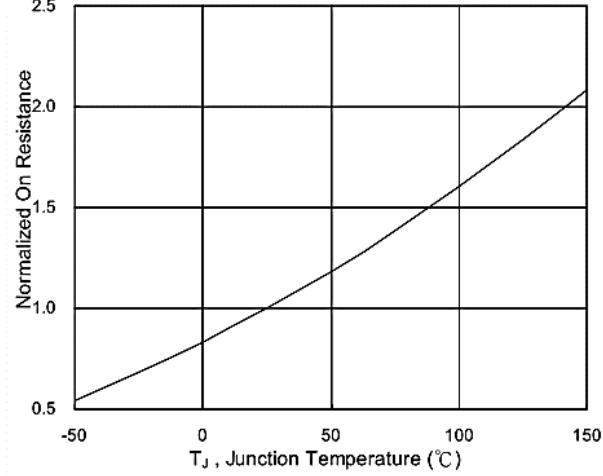


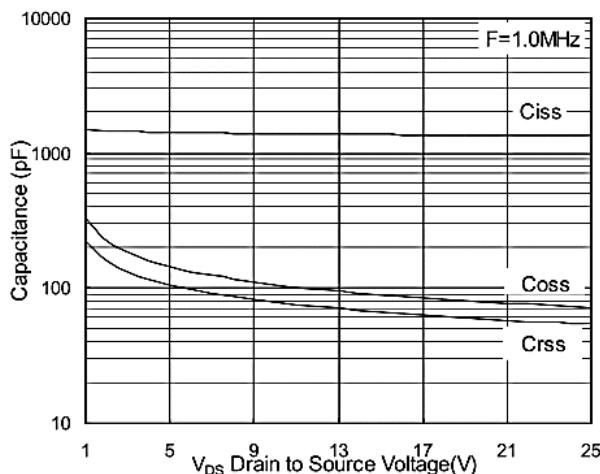
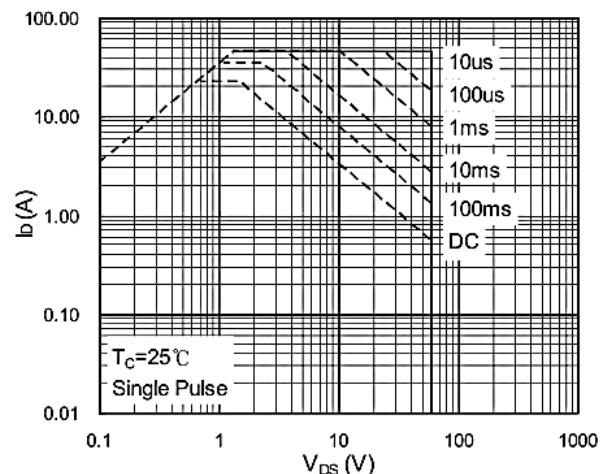
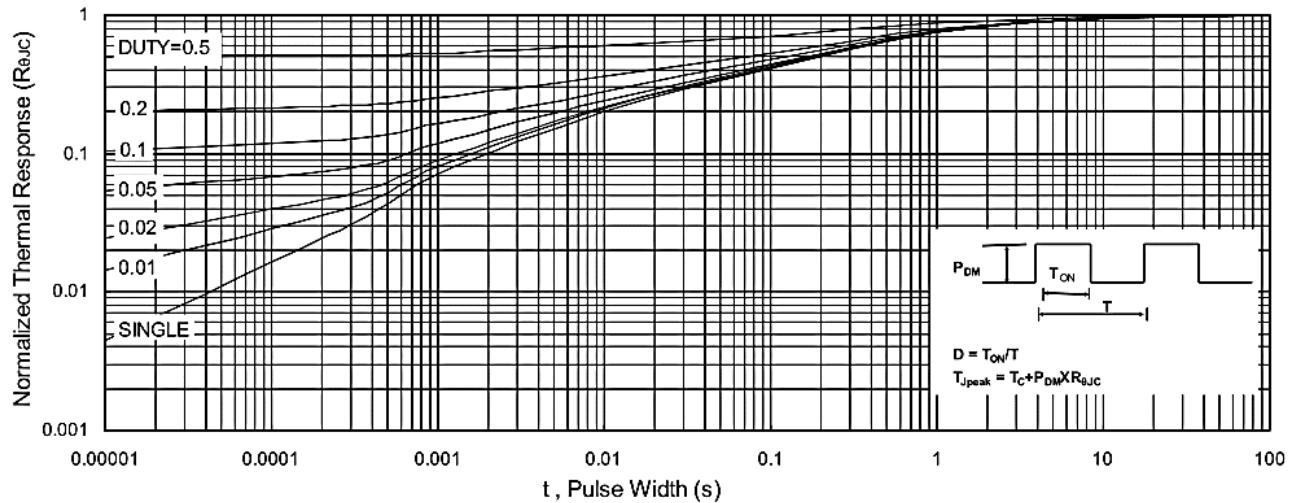
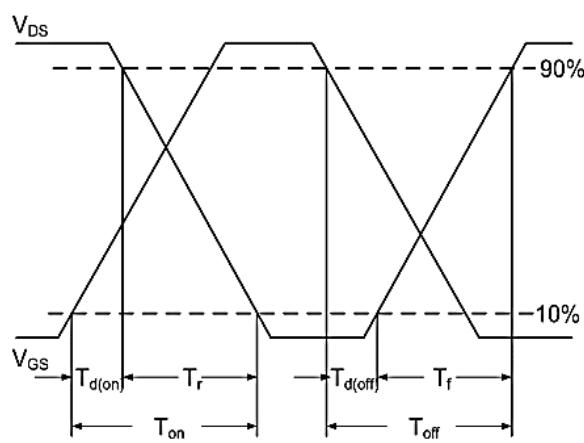
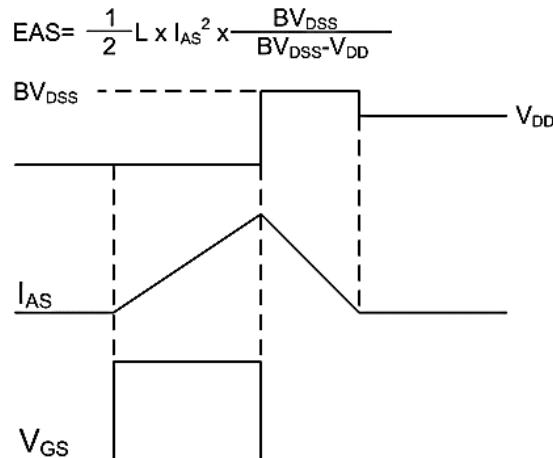
60V N-Channel Enhancement Mode MOSFET
Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

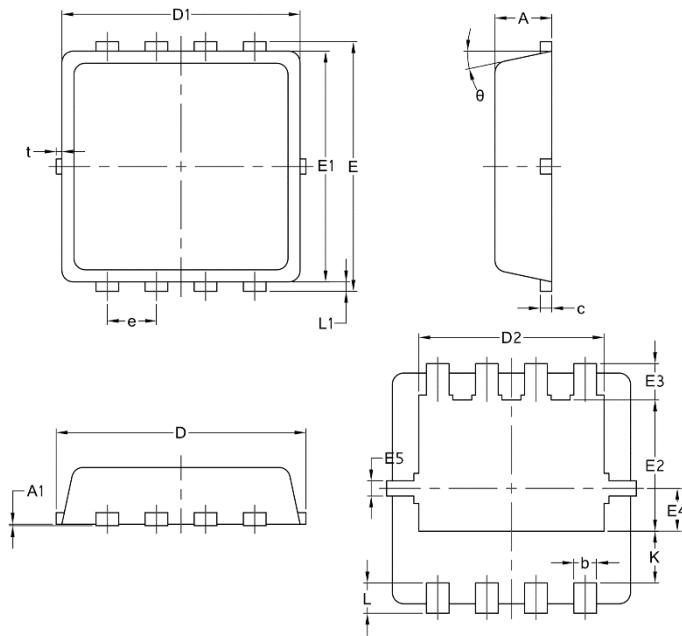
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	60	65	---	V
$\Delta BVDSS/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.063	---	$\text{V}/^{\circ}\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=15\text{A}$	---	20	32	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$	---	30	38	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.2	1.6	2.5	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	-5.24	---	$\text{mV}/^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=48\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=48\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=15\text{A}$	---	17	---	S
R _g	Gate Resistance	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	3.2	---	Ω
Q _g	Total Gate Charge (4.5V)	$V_{DS}=48\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=12\text{A}$	---	12.6	---	nC
Q _{gs}	Gate-Source Charge		---	3.2	---	
Q _{gd}	Gate-Drain Charge		---	6.3	---	
Td(on)	Turn-On Delay Time	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\Omega$, $I_D=10\text{A}$	---	8	---	ns
T _r	Rise Time		---	14.2	---	
Td(off)	Turn-Off Delay Time		---	24.4	---	
T _f	Fall Time		---	4.6	---	
C _{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	1378	---	pF
C _{oss}	Output Capacitance		---	86	---	
C _{rss}	Reverse Transfer Capacitance		---	64	---	
I _s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	23	A
ISM	Pulsed Source Current ^{2,5}		---	---	46	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $VDD=25\text{V}$, $VGS=10\text{V}$, $L=0.1\text{mH}$, $IAS=22\text{A}$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance v.s Gate-Source

Fig.3 Forward Characteristics of Reverse

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized V_{GS(th)} v.s T_J

Fig.6 Normalized R_{DS(on)} v.s T_J

60V N-Channel Enhancement Mode MOSFET

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Waveform

Package Mechanical Data-DFN3*3-8L-JQ Single


Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14