## **60V N-Channel Enhancement Mode MOSFET**

Q D

#### **Description**

The AP30N06DF uses advanced trench technology to provide excellent R<sub>DS(ON)</sub>, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

V<sub>DS</sub> = 60V I<sub>D</sub> =30A

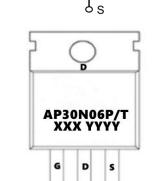
 $R_{DS(ON)}$  <36m $\Omega$  @  $V_{GS}$ =10V (Type: 28m $\Omega$ )

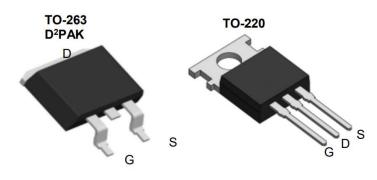
#### **Application**

LED lamp

Load switch

Uninterruptible power supply





**Package Marking and Ordering Information** 

Product ID	Pack	Marking	Qty(PCS)
AP30N06P	TO-220-3L	AP30N06P XXX YYYY	1000
AP30N06T	TO-263-3L	AP30N06T XXX YYYY	800

Symbol	Parameter	Max.	Units
VDSS	Drain-Source Voltage	60	V
VGSS	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	30	А
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	16	A
IDM	Pulsed Drain Current	74	А
IAS	Avalanche Current	13	A
EAS	Single Pulsed Avalanche Energy	22	mJ
P <sub>D</sub> @T <sub>C</sub> =25°C	Power Dissipation	31.3	W
TJ, TSTG	Operating and Storage Temperature Range	-55 to +175	°C
ReJA	Thermal Resistance Junction-Ambient <sup>1</sup>	62.5	°C/W
R₀JC	Thermal Resistance Junction-Case <sup>1</sup>	4	°C/W



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#### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	60	65		V
∆BVDSS/∆TJ	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.044		V/°C
		V <sub>GS</sub> =10V , I <sub>D</sub> =15A		28	36	mΩ
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =7A		38	45	mΩ
VGS(th)	Gate Threshold Voltage		1.2	1.6	2.5	V
$\Delta V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=250uA$		-4.8		mV/°C
IDSS	Drain Source Leakage Current	V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	
1033	Drain-Source Leakage Current	V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	uA
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =15A		25.3		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.5		Ω
Qg	Total Gate Charge (10V)			19		
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =48V , V <sub>GS</sub> =10V , I <sub>D</sub> =15A	1	2.5		nC
$Q_{gd}$	Gate-Drain Charge			5		
Td(on)	Turn-On Delay Time			2.8		
Tr	Rise Time	$V_{DD}$ =30V , $V_{GS}$ =10V , $R_{G}$ =3.3 $\Omega$		16.6		ne
Td(off)	Turn-Off Delay Time	I <sub>D</sub> =15A	-	21.2		ns
T <sub>f</sub>	Fall Time			5.6		
C <sub>iss</sub>	Input Capacitance		I	1027		
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz	I	65		pF
Crss	Reverse Transfer Capacitance		I	46		
Is	Continuous Source Current <sup>1,6</sup>	\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\			20	Α
ISM	Pulsed Source Current <sup>2,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	-		40	Α
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C	-		1.2	V
t <sub>rr</sub>	Reverse Recovery Time	IF=15A , dI/dt=100A/μs ,		12.2		nS
Q <sub>rr</sub>	Reverse Recovery Charge	TJ=25°C		7.3		nC

#### Note:

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- $\ensuremath{\mathsf{2}}_{\ensuremath{\mathsf{N}}}$  The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3. The test cond  $\leq$  300us duty cycle  $\leq$  2%, duty cycle ition is TJ =25°C, VDD =48V, VG =10V, RG =25 $\Omega$ , L=0.1mH, IAS =13A
- 5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

## **60V N-Channel Enhancement Mode MOSFET**

### **Typical Characteristics**

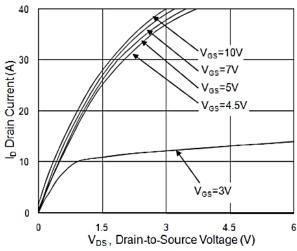


Fig.1 Typical Output Characteristics

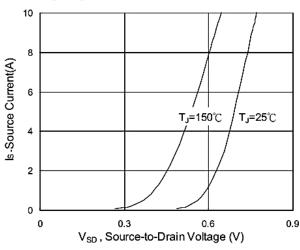


Fig.3 Forward Characteristics Of Reverse

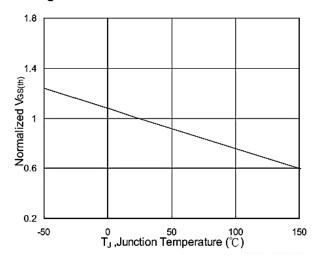


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$ 

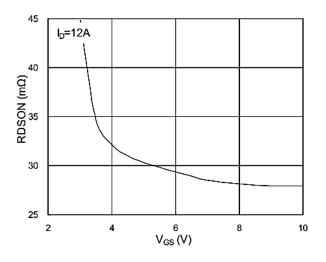


Fig.2 On-Resistance vs. Gate-Source

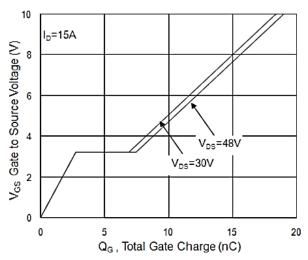


Fig.4 Gate-Charge Characteristics

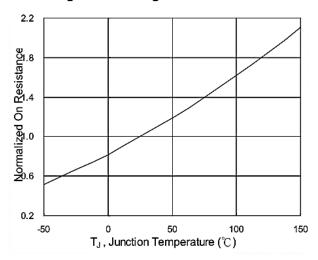
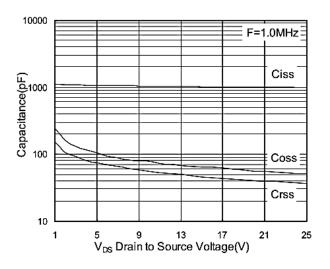


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>

## **60V N-Channel Enhancement Mode MOSFET**



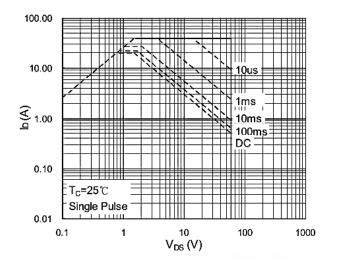


Fig.7 Capacitance

Fig.8 Safe Operating Area

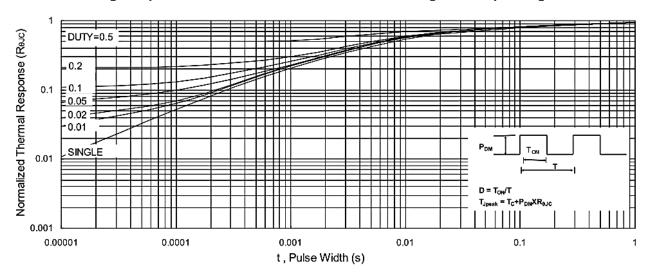
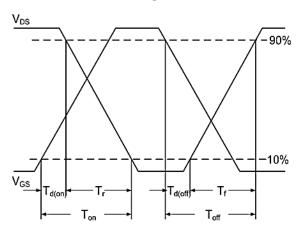
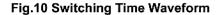


Fig.9 Normalized Maximum Transient Thermal Impedance





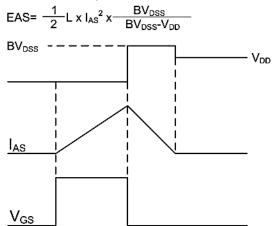
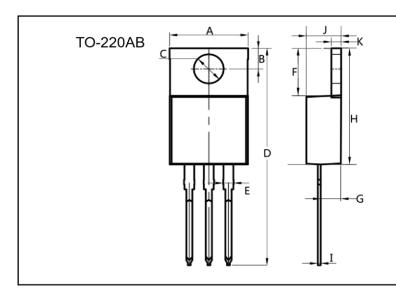
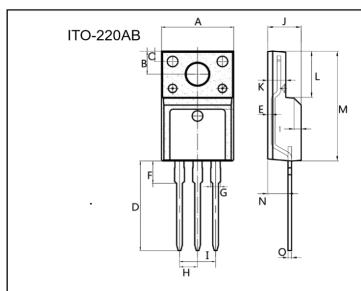


Fig.11 Unclamped Inductive Switching Waveform

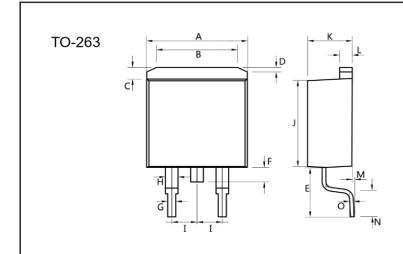
## **60V N-Channel Enhancement Mode MOSFET**



Dim.	Min.	Max.	
Α	10.0	10.4	
В	2.5	3.0	
С	3.5	4.0	
D	28.0	30.0	
E	1.1	1.5	
F	6.2	6.6	
G	2.9	3.3	
Н	15.0	16.0	
I	0.35	0.45	
J	4.3	4.7	
K	1.2	1.4	
All Dimensions in millimeter			



Dim.	Min. Max.		
Α	9.9	10.3	
В	2.9	3.5	
С	1.15	1.45	
D	12.75	13.25	
E	0.55	0.75	
F	3.1	3.5	
G	1.25	1.45	
Н	Typ 2.54		
I	Typ 5.08		
J	4.55	4.75	
K	2.4	2. 7	
L	6.35	6.75	
M	15.0	16.0	
N	2.75	3.15	
0	0.45	0.60	
All Dimensions in millimeter			



Dim.	Min.	Max.	
Α	10.0	10. 5	
В	7.25	7.75	
С	1.3	1.5	
D	0.55	0.75	
E	5.0	6.0	
F	1.4	1.6	
G	0.75	0.95	
Н	1.15	1.35	
I	Typ 2.54		
J	8.4	8.6	
K	4.4	4.6	
L	1.25	1.45	
M	0.02	0.1	
N	2.4	2.8	
0	0.35	0.45	
All Dimensions in millimeter			