### **60V N-Channel Enhancement Mode MOSFET**

#### **Description**

The AP12N06S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = 60V I_{D} = 12A$ 

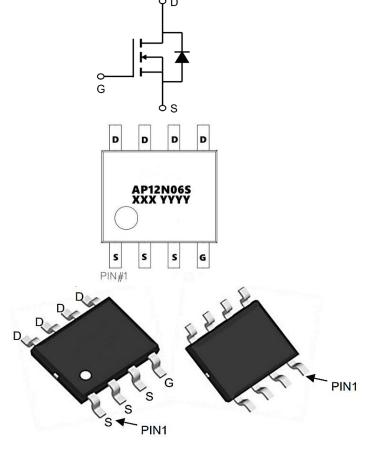
 $R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=10V$  (Type: 24m $\Omega$ )

#### **Application**

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

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Product ID	Pack	Marking	Qty(PCS)	
AP12N06S	SOP-8L	AP12N06S XXX YYYY	3000	

### Absolute Maximum Ratings (T<sub>C</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units	
V <sub>D</sub> S	Drain-Source Voltage	60	V	
V <sub>G</sub> s	Gate-Source Voltage	±20	V	
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	12	A	
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	inuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup> 11		
Ідм	Pulsed Drain Current <sup>2</sup>	Pulsed Drain Current <sup>2</sup> 36		
EAS	Single Pulse Avalanche Energy <sup>3</sup>	25.5	mJ	
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	34.7	W	
Тѕтс	Storage Temperature Range	-55 to 150	°C	
TJ	Operating Junction Temperature Range	-55 to 150	°C	
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	°C/W	
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	28 °C/W		



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### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	60	65		V	
∆BVDSS/∆TJ	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.063		V/°C	
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =15A		24	32	mΩ	
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =10A		33	42		
VGS(th)	Gate Threshold Voltage	\/ -\/   -250\	1.2	1.6	2.5	V	
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	$V_{GS}=V_{DS}$ , $I_D=250uA$		-5.24		mV/°C	
IDCC	Drain-Source Leakage Current	V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA	
IDSS		V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5		
IGSS	Gate-Source Leakage Current	$V_{GS}$ =±20 $V$ , $V_{DS}$ =0 $V$			±100	nA	
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =15A		17		S	
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		3.2		Ω	
$Q_g$	Total Gate Charge (4.5V)			12.6			
Qgs	Gate-Source Charge	V <sub>DS</sub> =48V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =12A		3.2		nC	
$Q_{gd}$	Gate-Drain Charge			6.3	I		
Td(on)	Turn-On Delay Time			8			
Tr	Rise Time	$V_{DD}$ =30V , $V_{GS}$ =10V , $R_{G}$ =3.3 $\Omega$ ,		14.2	-	] ,,,	
Td(off)	Turn-Off Delay Time	I <sub>D</sub> =10A		24.4		ns -	
T <sub>f</sub>	Fall Time			4.6			
C <sub>iss</sub>	Input Capacitance			1378			
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		86		pF	
Crss	Reverse Transfer Capacitance			64			
Is	Continuous Source Current <sup>1,5</sup>	\/-=\/-=0\/ Force Cument			23	Α	
ISM	Pulsed Source Current <sup>2,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			46	Α	
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V	

#### Note:

- 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2 、The data tested by pulsed , pulse width  $\leqq 300 us$  , duty cycle  $\leqq 2\%$
- 3. The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

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#### **Typical Characteristics**

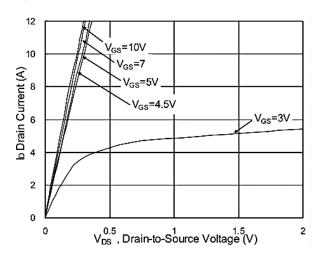


Fig.1 Typical Output Characteristics

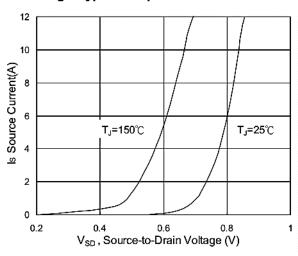


Fig.3 Forward Characteristics of Reverse

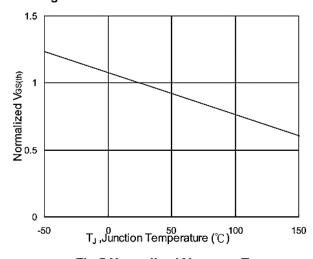


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$ 

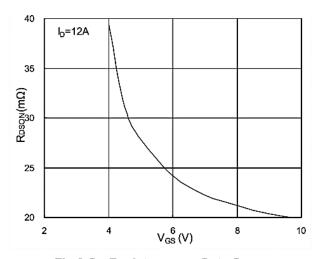


Fig.2 On-Resistance v.s Gate-Source

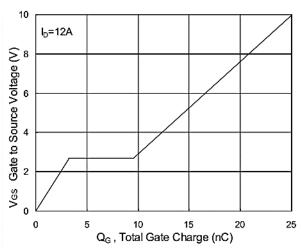


Fig.4 Gate-Charge Characteristics

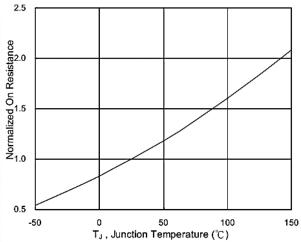
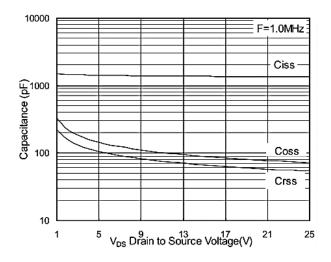


Fig.6 Normalized  $R_{DSON}$  v.s  $T_J$ 

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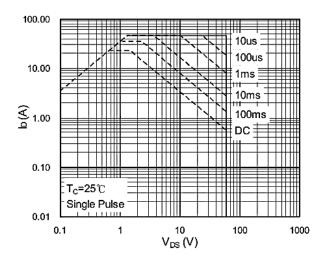


Fig.7 Capacitance

Fig.8 Safe Operating Area

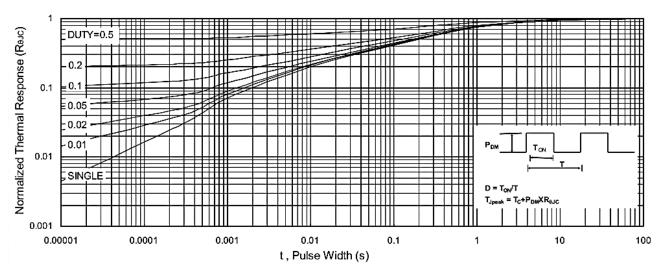


Fig.9 Normalized Maximum Transient Thermal Impedance

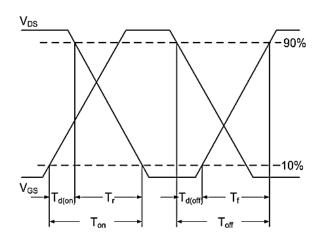


Fig.10 Switching Time Waveform

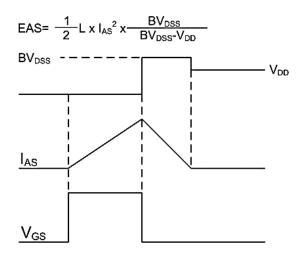
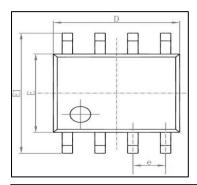


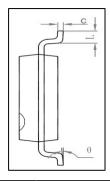
Fig.11 Unclamped Inductive Waveform

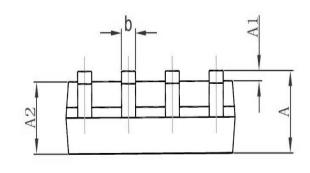


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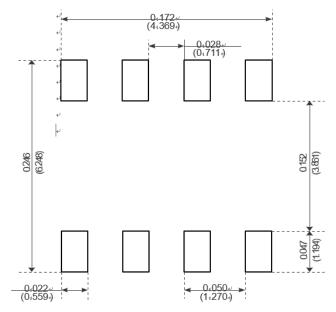
## Package Mechanical Data-SOP-8







Ch - 1	Dimensions Ir	n Millimeters	Dimensions	In Inches
Symbol	Min	Max	Min	Max
Α	1. 350	1. 750	0. 053	0.069
A1	0. 100	0. 250	0. 004	0. 010
A2	1. 350	1. 550	0. 053	0. 061
b	0. 330	0. 510	0. 013	0. 020
С	0. 170	0. 250	0.006	0. 010
D	4. 700	5. 100	0. 185	0. 200
E	3. 800	4. 000	0. 150	0. 157
E1	5. 800	6. 200	0. 228	0. 244
е	1. 270 (BSC)		0. 050 (BSC)	
L	0. 400	1. 270	0. 016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads-