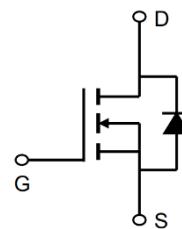


## Description

The AP75N04NF uses advanced **SGT V** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

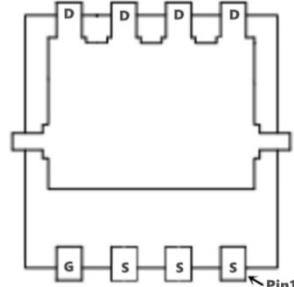


## General Features

$V_{DS} = 40V$   $I_D = 75A$

$R_{DS(ON)} < 5.5m\Omega$  @  $V_{GS}=10V$  (**Type: 4.5mΩ**)

$C_{iss} \approx 1204\text{ PF}$

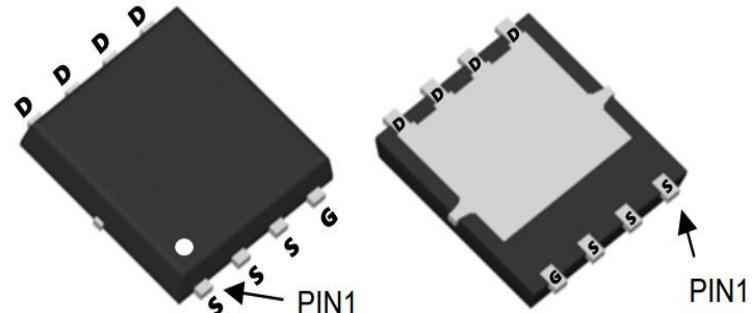


## Application

Wireless charging

Boost driver

Brushless motor



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP75N04NF	PDFN5*6-8L	AP75N04NF XXX YYYY	5000

## Absolute Maximum Ratings ( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	75	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	44	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	250	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	36	mJ
$I_{AS}$	Avalanche Current	27	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	42	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	25	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	3.0	°C/W



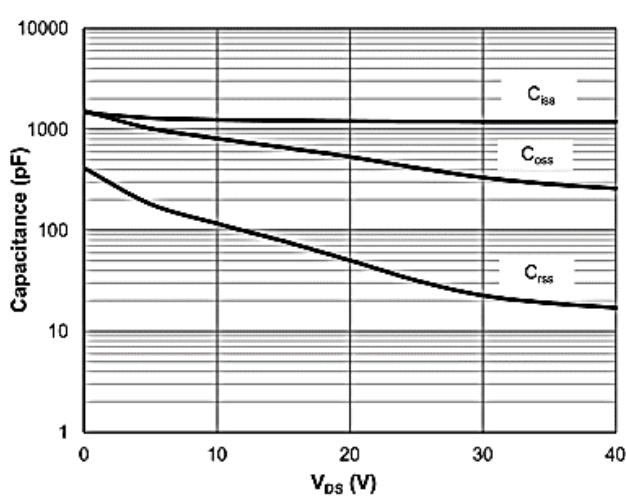
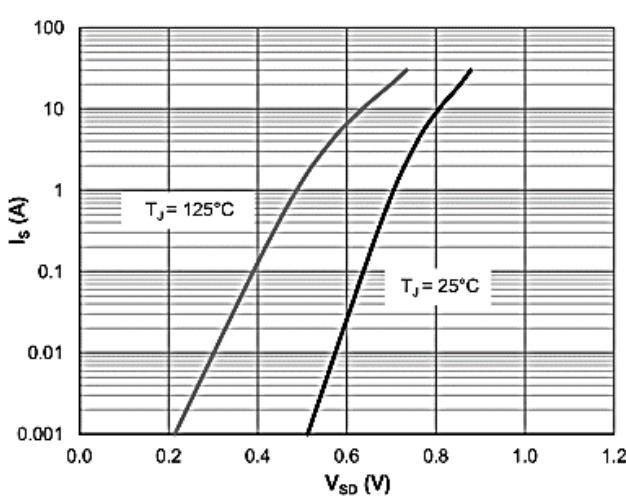
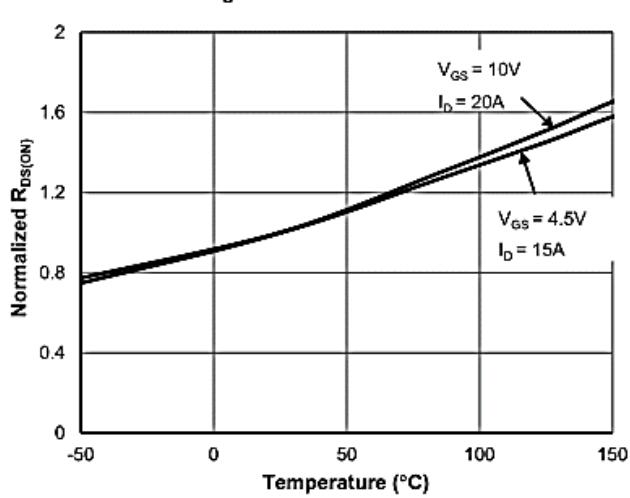
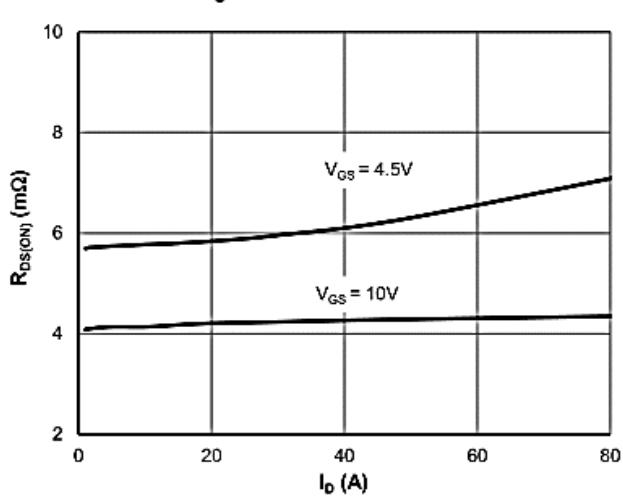
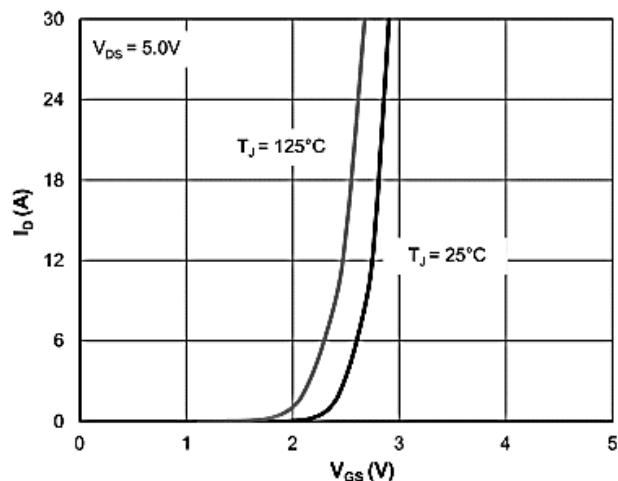
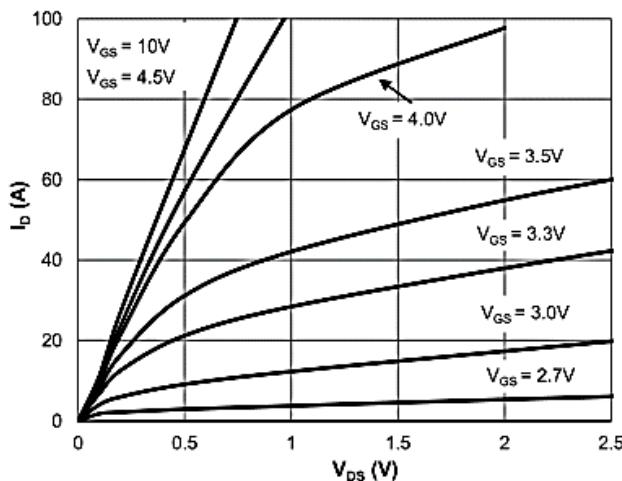
**40V N-Channel Enhancement Mode MOSFET**
**N-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

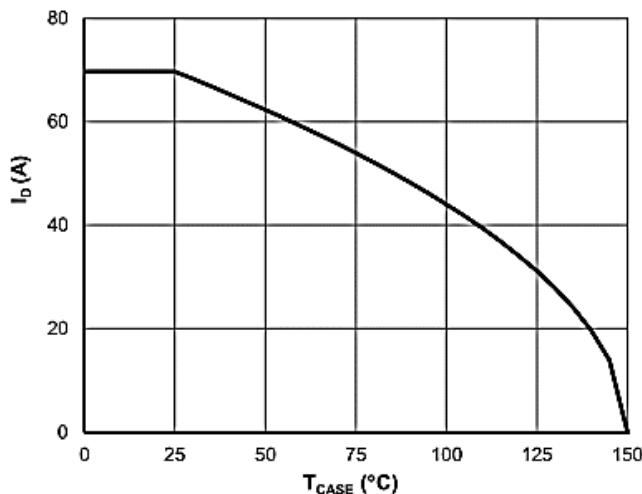
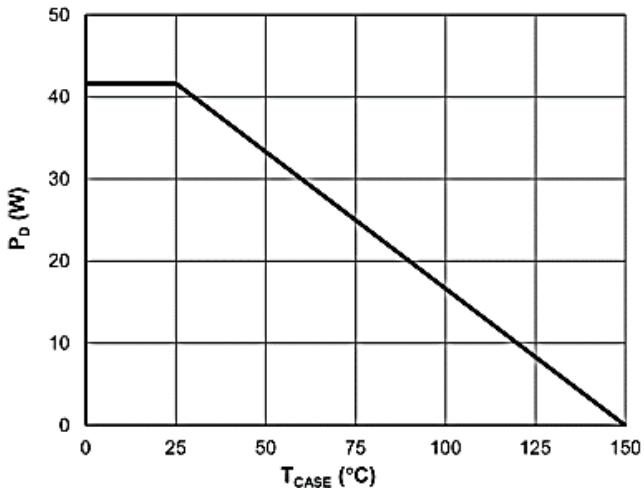
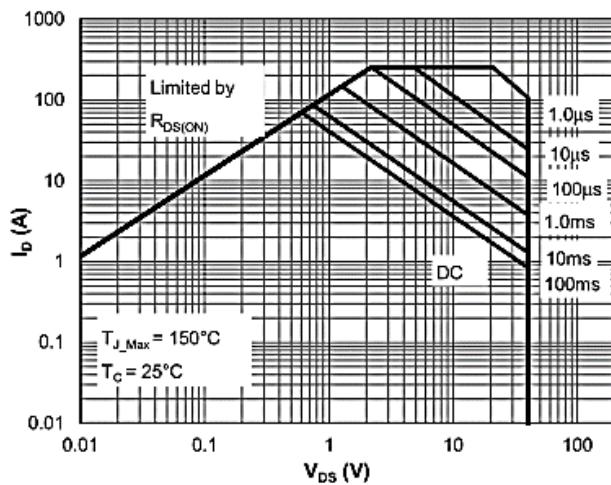
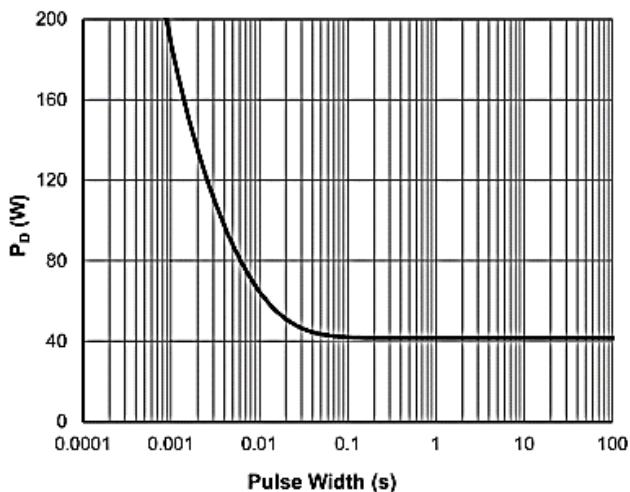
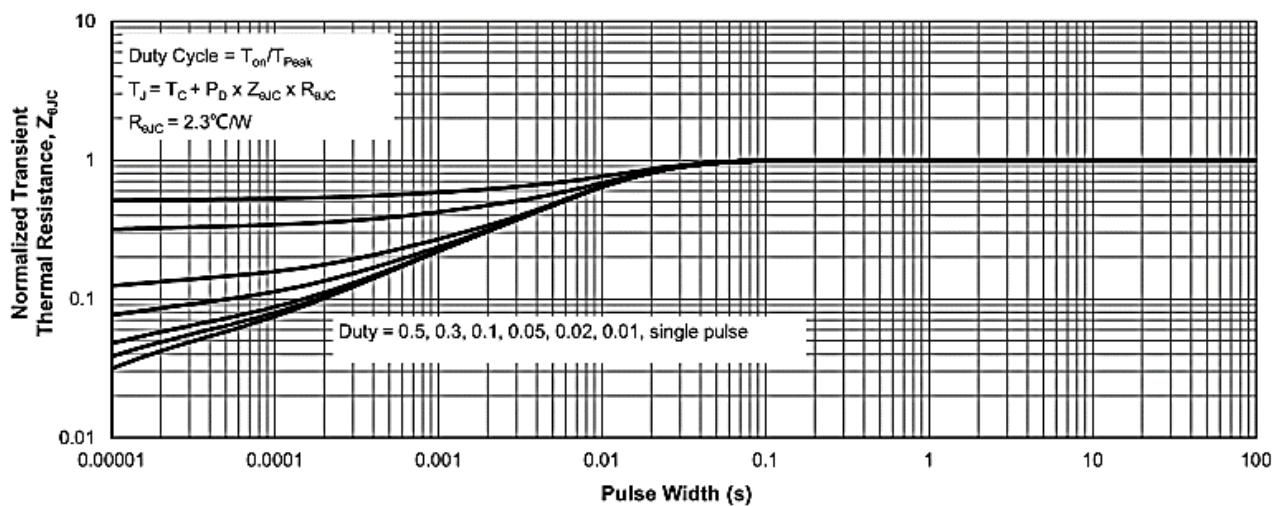
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	40	47	---	V
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10\text{V}$ , $I_D=30\text{A}$	---	4.5	5.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=20\text{A}$	---	5.8	7.6	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250\mu\text{A}$	1.2	1.6	2.5	V
IDSS	Drain-Source Leakage Current	$V_{DS}=32\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$	---	---	1	$\text{uA}$
		$V_{DS}=32\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm20\text{V}$ , $V_{DS}=0\text{V}$	---	---	$\pm100$	nA
$R_g$	Gate Resistance	$V_{DS}=0\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	---	1.8	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=20\text{V}$ , $V_{GS}=4.5\text{V}$ , $I_D=12\text{A}$	---	9.7	---	$\text{nC}$
$Q_{gs}$	Gate-Source Charge		---	3.2	---	
$Q_{gd}$	Gate-Drain Charge		---	4.0	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15\text{V}$ , $V_{GS}=10\text{V}$ , $R_G=3.3\Omega$ $I_D=1\text{A}$	---	4.8	---	$\text{ns}$
$T_r$	Rise Time		---	8.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	23	---	
$T_f$	Fall Time		---	15.2	---	
$C_{iss}$	Input Capacitance	$V_{DS}=20\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	---	1204	---	$\text{pF}$
$C_{oss}$	Output Capacitance		---	536	---	
$C_{rss}$	Reverse Transfer Capacitance		---	51	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0\text{V}$ , Force Current	---	---	42	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0\text{V}$ , $I_S=1\text{A}$ , $T_J=25^\circ\text{C}$	---	---	1.0	V

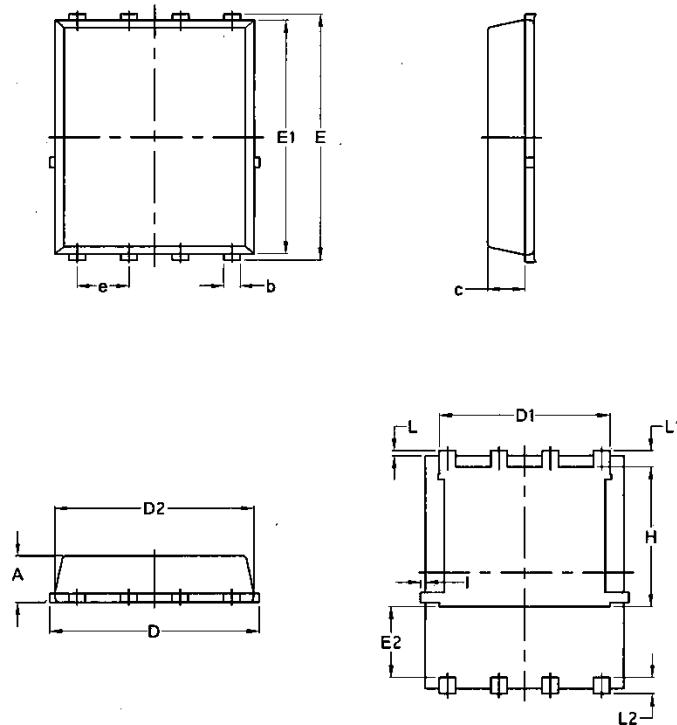
**Note :**

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is  $VDD =32\text{V}$ , $VGS =10\text{V}$ , $L=0.1\text{mH}$ , $IAS =27\text{A}$
- 4、The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

### Typical Characteristics



**40V N-Channel Enhancement Mode MOSFET**

**Figure 7: Current De-rating**

**Figure 8: Power De-rating**

**Figure 9: Maximum Safe Operating Area**

**Figure 10: Single Pulse Power Rating, Junction-to-Case**

**Figure 11: Normalized Maximum Transient Thermal Impedance**

**Package Mechanical Data-PDFN5\*6-8L-JQ Single**


Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070