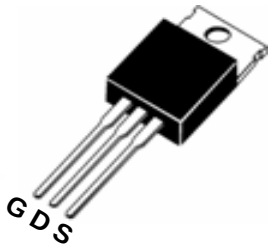
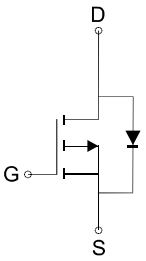
P-Channel 100V(D-S) MOSFET

The FIR16P10PG is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

PIN Connection TO-220AB





P-Channel MOSFET

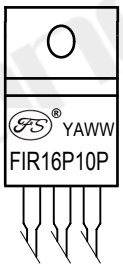
FEATURES

- $R_{DS(ON)} \leqq 195m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 210m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
FIR16P10P = Specific Device Code

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	-11	A
	T_C=70℃		-9	
Pulsed Drain Current		I_{DM}	-44	A
Maximum Power Dissipation*	T_C=25℃	P_D	39	W
	T_C=70℃		25	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	3.2	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

Electrical Characteristics (Tc =25℃ Unless Otherwise Specified)

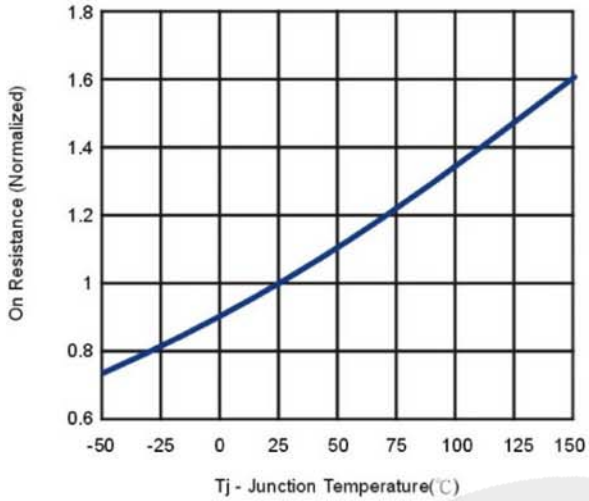
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±250	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -3.6A		160	195	mΩ
		V_{GS}=-4.5V, I_D= -3.4A		170	210	
V_{SD}	Diode Forward Voltage	I_S=-2.9A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-50V, V_{GS}=-10V, I_D=-3.6A		28		nC
Qg	Total Gate Charge	V_{DS}=-50V, V_{GS}=-4.5V, I_D=-3.6A		14		
Qgs	Gate-Source Charge			5.3		
Qgd	Gate-Drain Charge			5.9		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, F=1MHz		1240		pF
Coss	Output Capacitance			947		
Crss	Reverse Transfer Capacitance			30		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-50V, R_L =25Ω V_{GEN}=-10V, R_G=1Ω		35		ns
t_r	Turn-On Rise Time			12		
$t_{d(off)}$	Turn-Off Delay Time			58		
t_f	Turn-On Fall Time			5		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

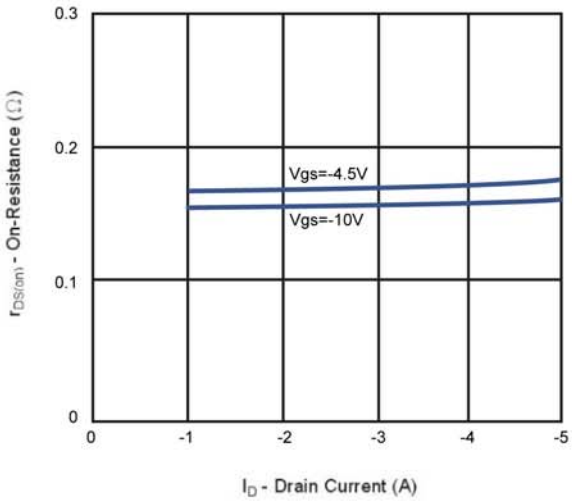
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J =25℃ Noted)

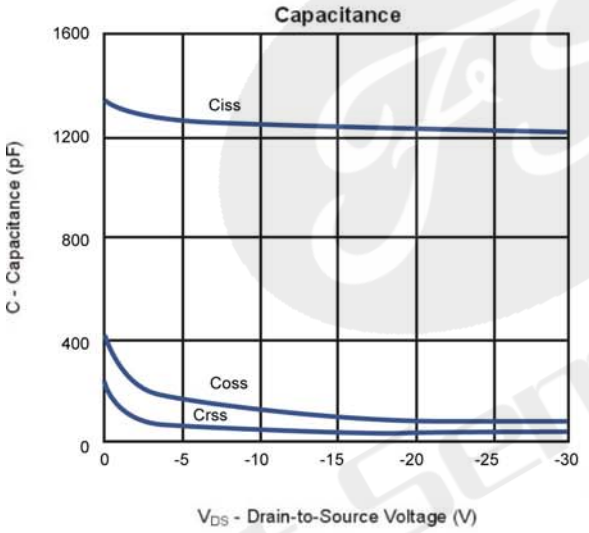
On Resistance vs. Junction Temperature



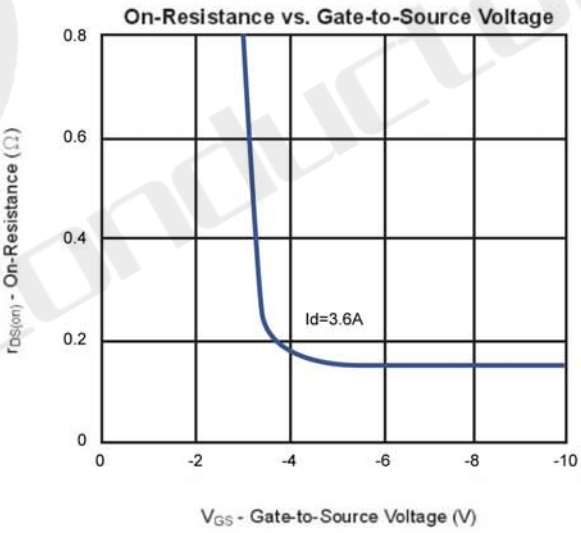
On-Resistance vs. Drain Current



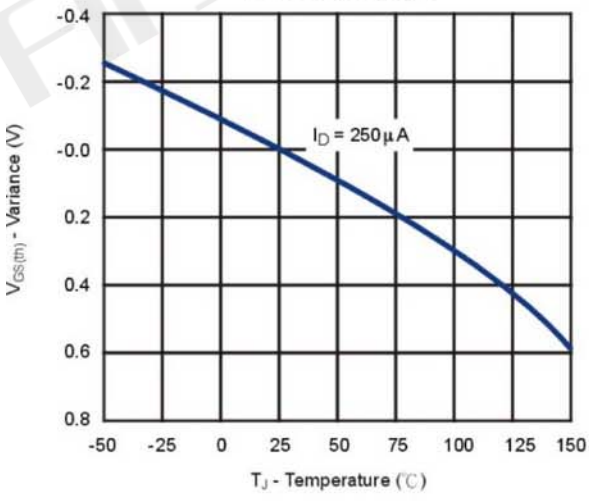
Capacitance



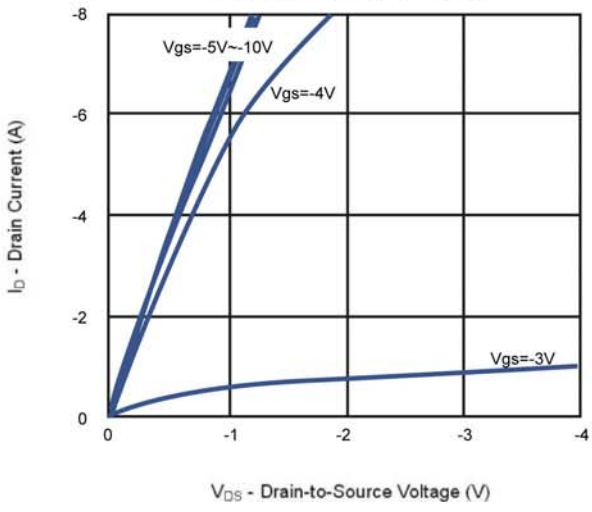
On-Resistance vs. Gate-to-Source Voltage



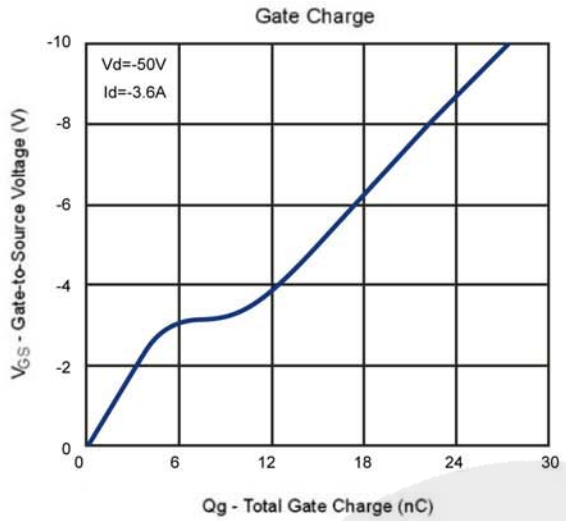
Threshold Voltage

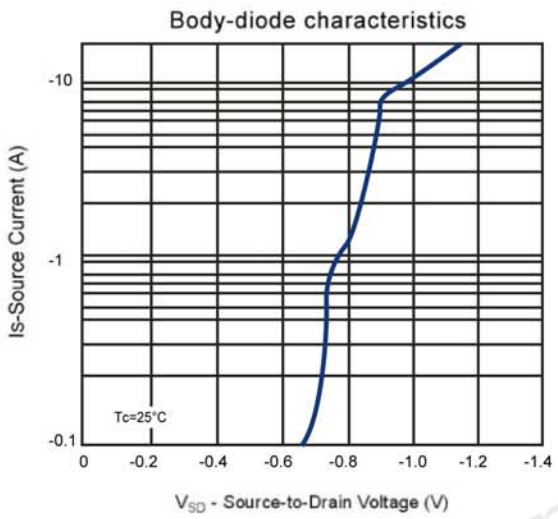


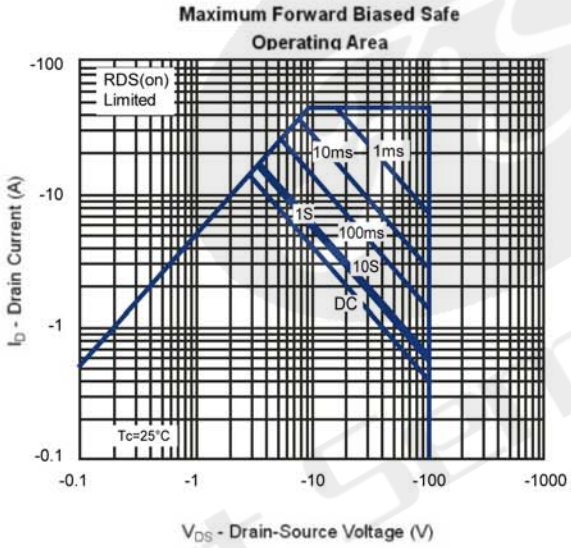
On-Region Characteristics

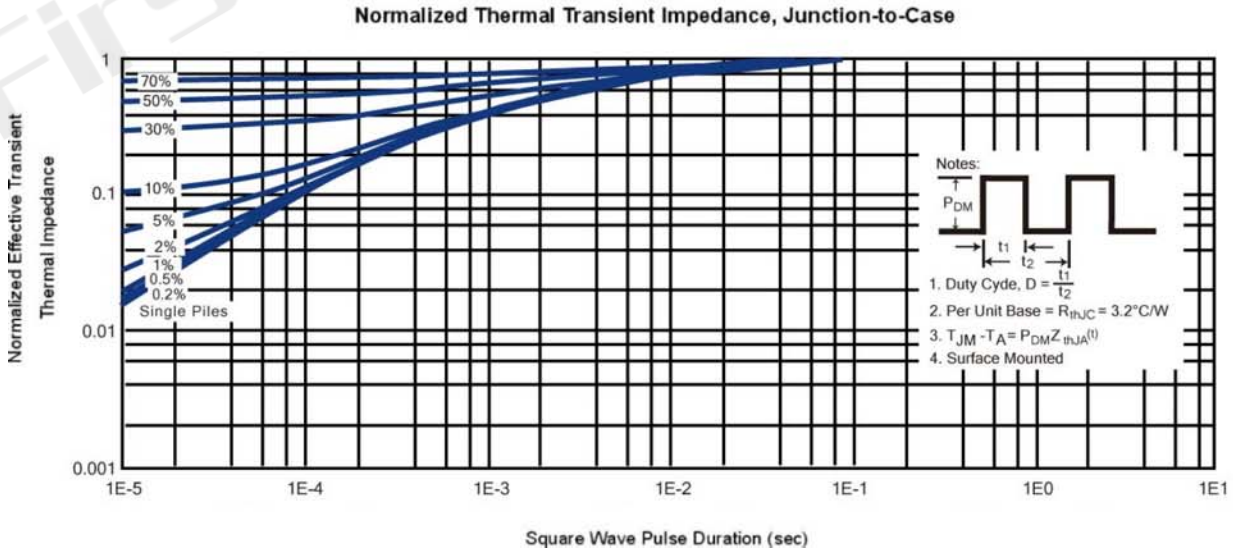


Typical Characteristics (T_J =25℃ Noted)

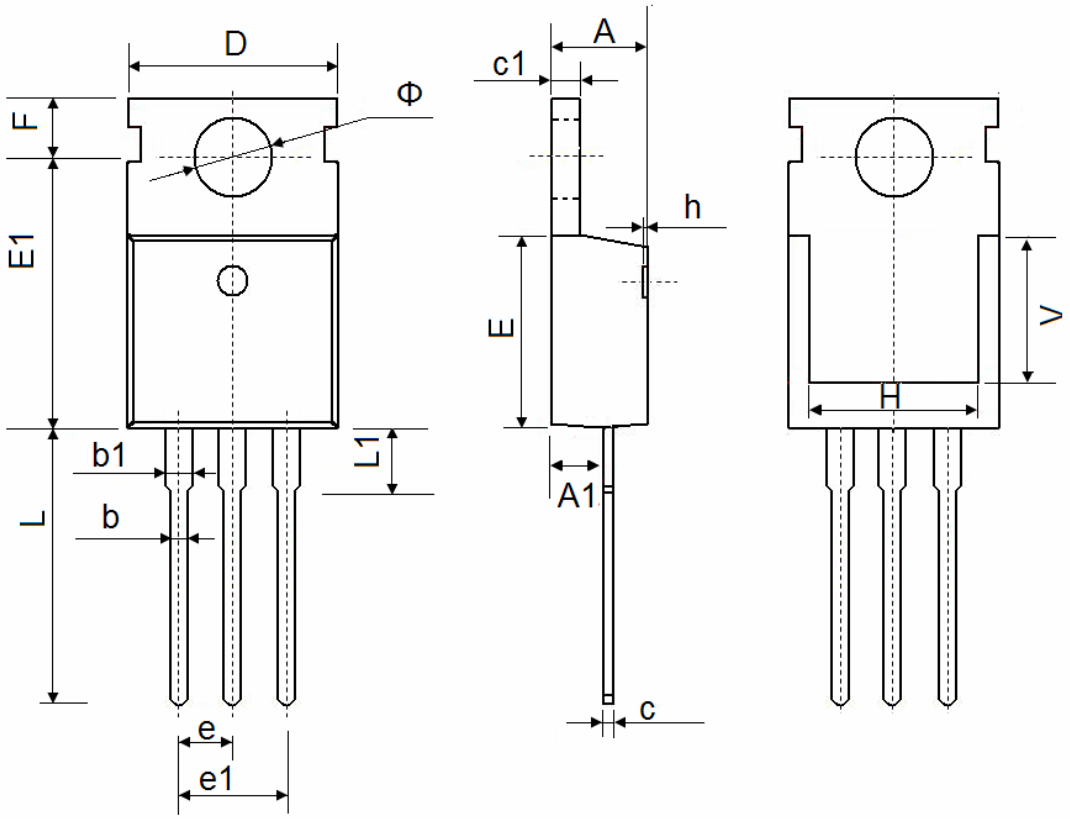








TO-220AB Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	