N-Channel 60V (D-S) MOSFET

Description

The FIR16N06DG uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

General Features

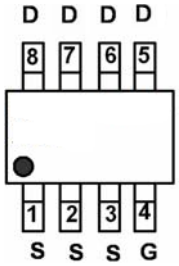
- V_{DS} =60V,I_D =16A
  $R_{DS(ON)}$=13mΩ (max) @ V_{GS}=10V
  $R_{DS(ON)}$=16mΩ (max) @ V_{GS}=4.5V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

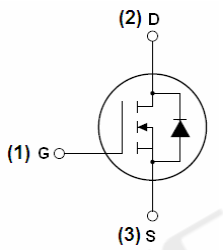
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

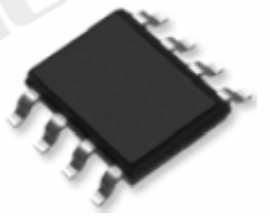
PIN CONFIGURATION

(SOP-8)





N-Channel MOSFET



SOP-8 top view

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	16	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	10.2	A
Pulsed Drain Current	I_{DM}	64	A
Maximum Power Dissipation	P_D	3.1	W
Derating factor		0.028	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	211	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient(Note 2)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

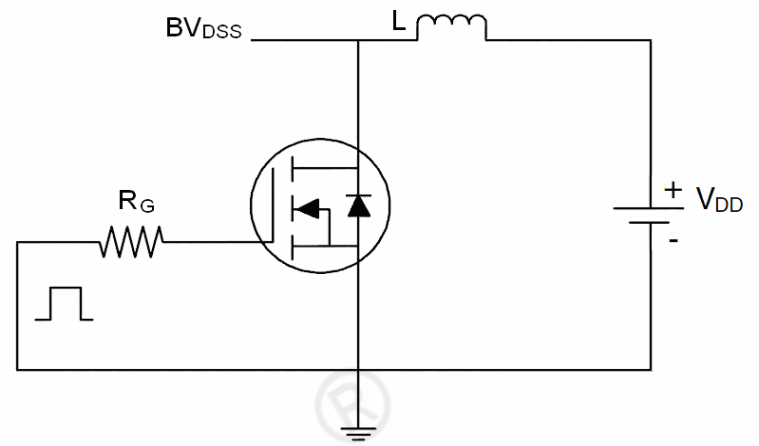
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	2	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=8A	-	10	13	mΩ
		V_{GS}=4.5V, I_D=8A	-	14	16	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=14A	45	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	4300	-	PF
Output Capacitance	C_{oss}		-	290	-	PF
Reverse Transfer Capacitance	C_{rss}		-	26	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V,I_D=14A V_{GS}=10V,R_G=1.6Ω	-	25	-	nS
Turn-on Rise Time	t_r		-	95	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	154	-	nS
Turn-Off Fall Time	t_f		-	77	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=14A, V_{GS}=10V	-	88	-	nC
Gate-Source Charge	Q_{gs}		-	17	-	nC
Gate-Drain Charge	Q_{gd}		-	15	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=14A	-	-	1.5	V
Diode Forward Current (Note 2)	I_S		-	-	16	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs(Note3)	-	73	-	nS
Reverse Recovery Charge	Qrr		-	15	-	nC

Notes:

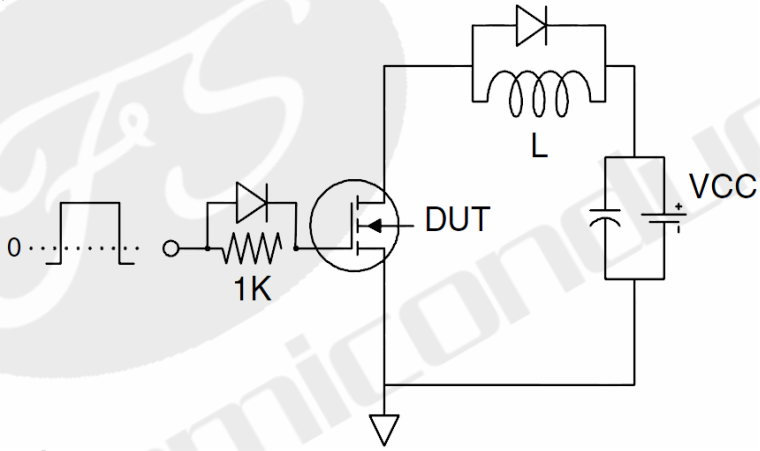
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit

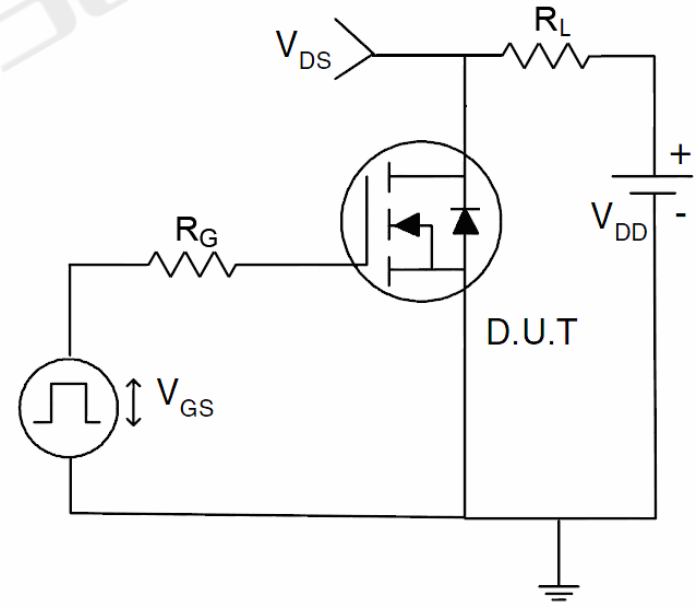


Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

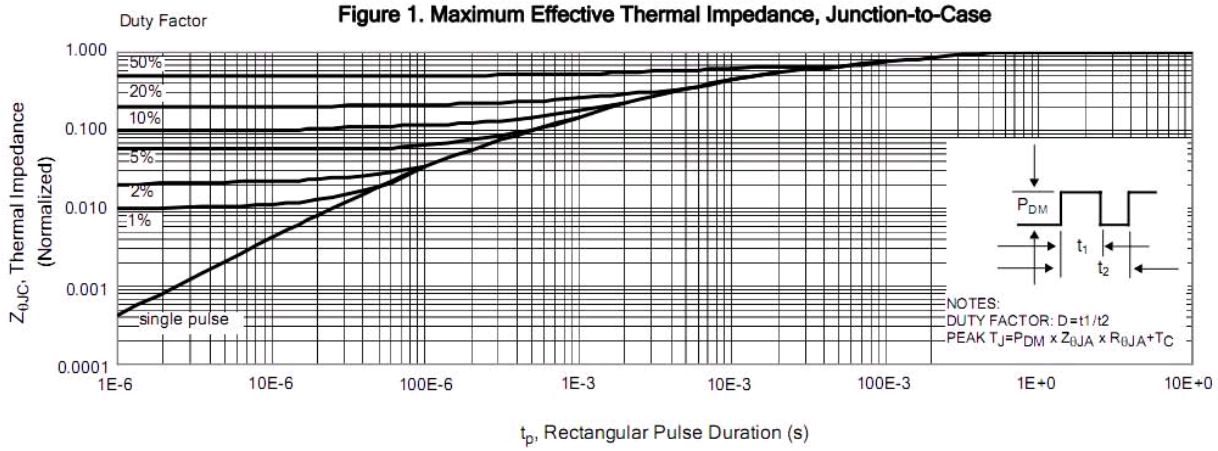


Figure 2. Maximum Power Dissipation

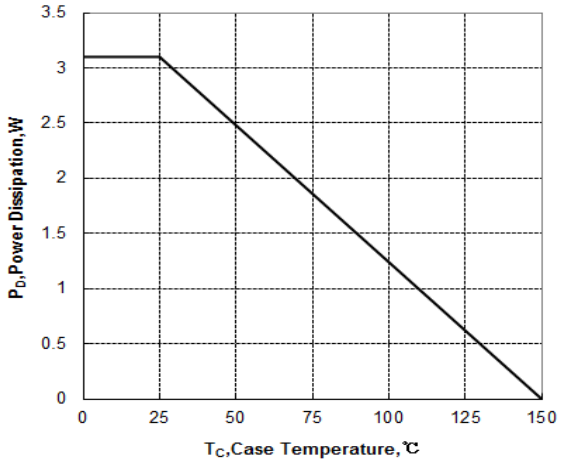


Figure3. Maximum Continuous Drain Current

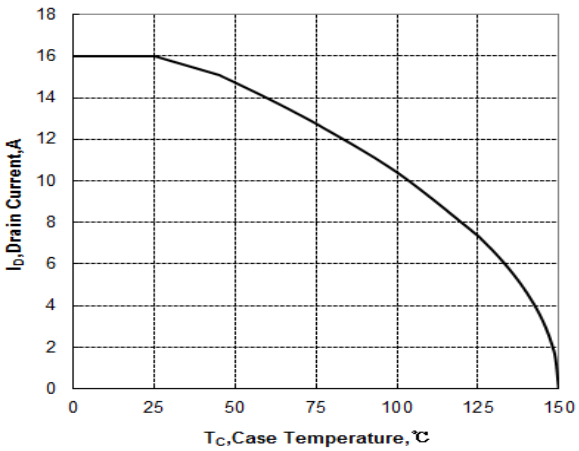


Figure 4. Typical Output Characteristics

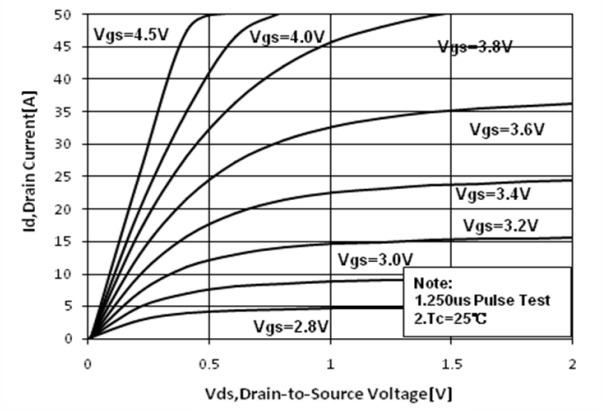


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

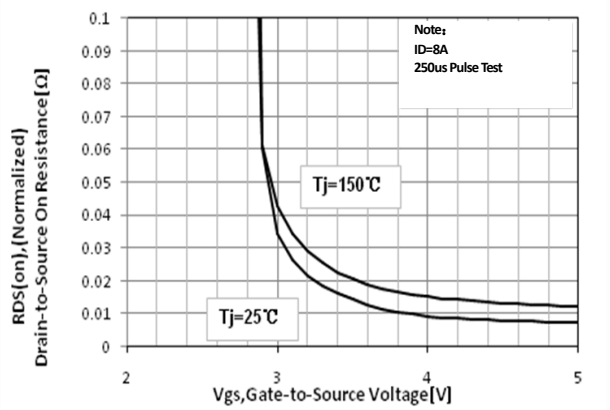


Figure 6. Typical Transfer Characteristics

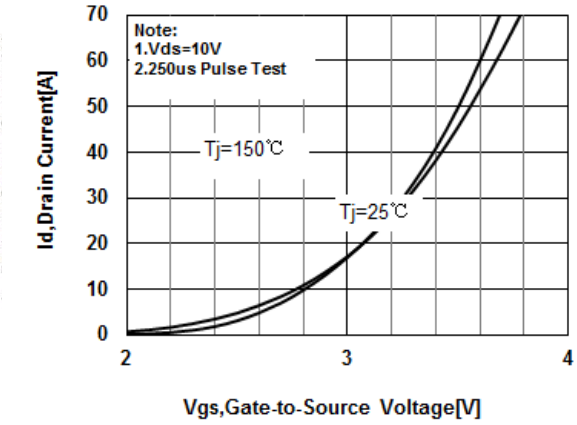


Figure 8. Typical Drain-to-Source ON Resistance vs Drain Current

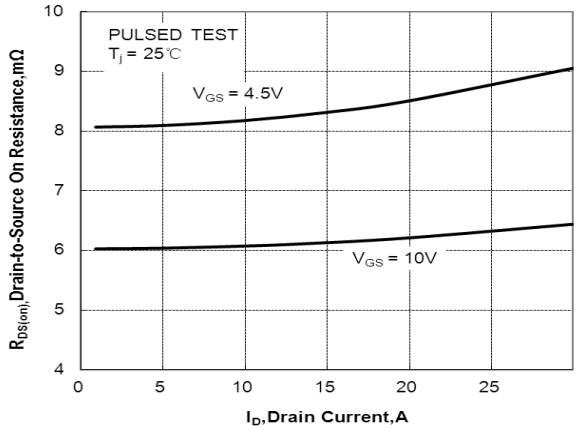


Figure 10. Typical Breakdown Voltage vs Junction Temperature

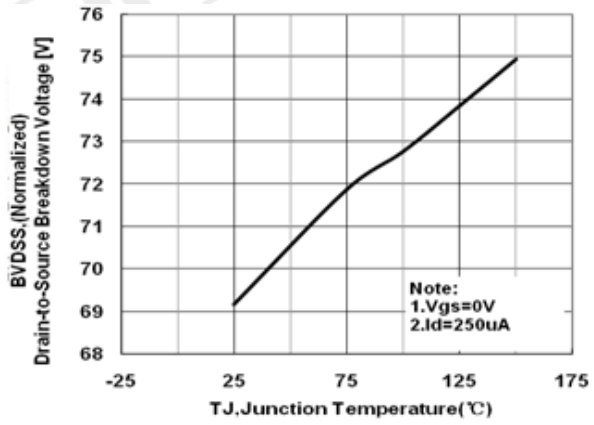


Figure8. Unclamped Inductive Switching Capability

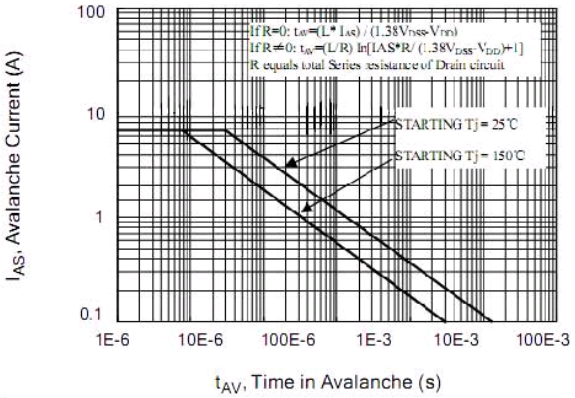


Figure 9. Drain-to-Source ON Resistance vs Junction Temperature

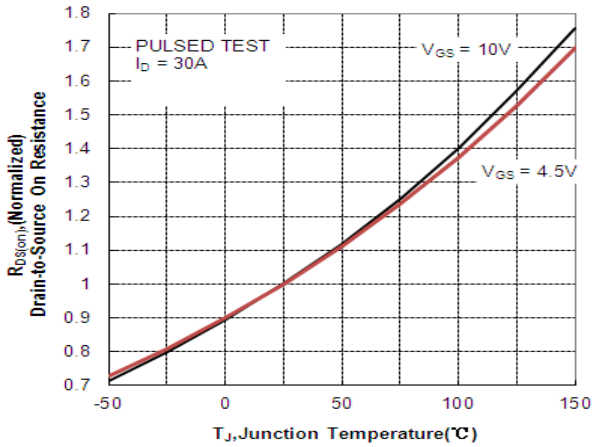


Figure 11. Typical Threshold Voltage vs Junction Temperature

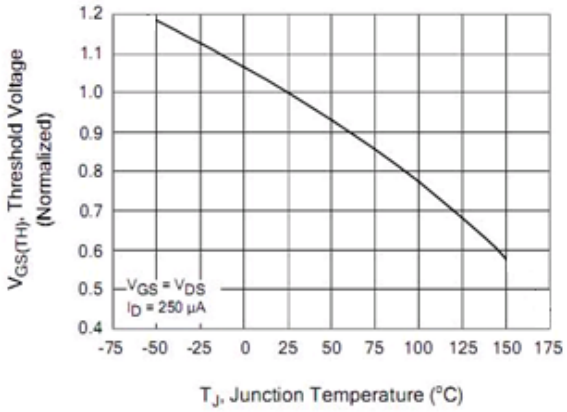


Figure 12.Maximum Forward Bias Safe Operating Area

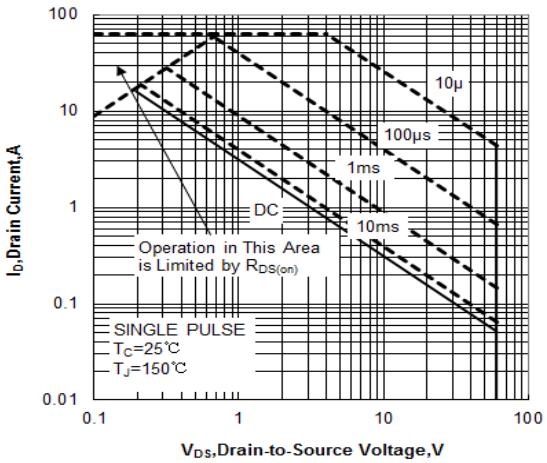


Figure 13. Typical Capacitance vs Drain-to-Source Voltage

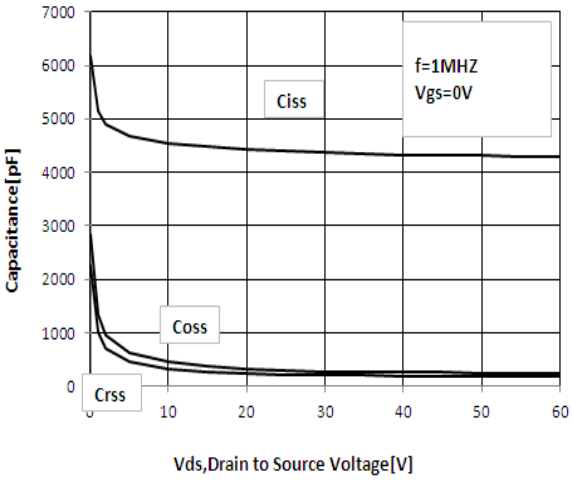
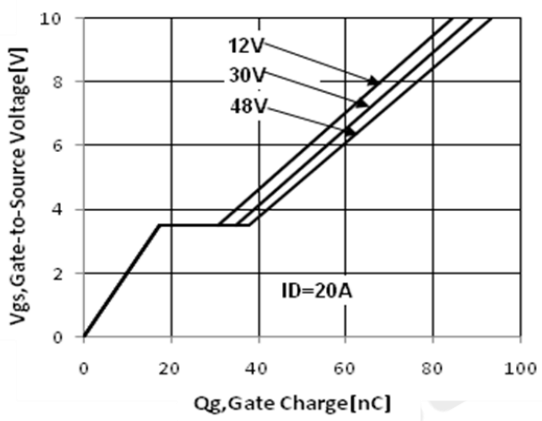
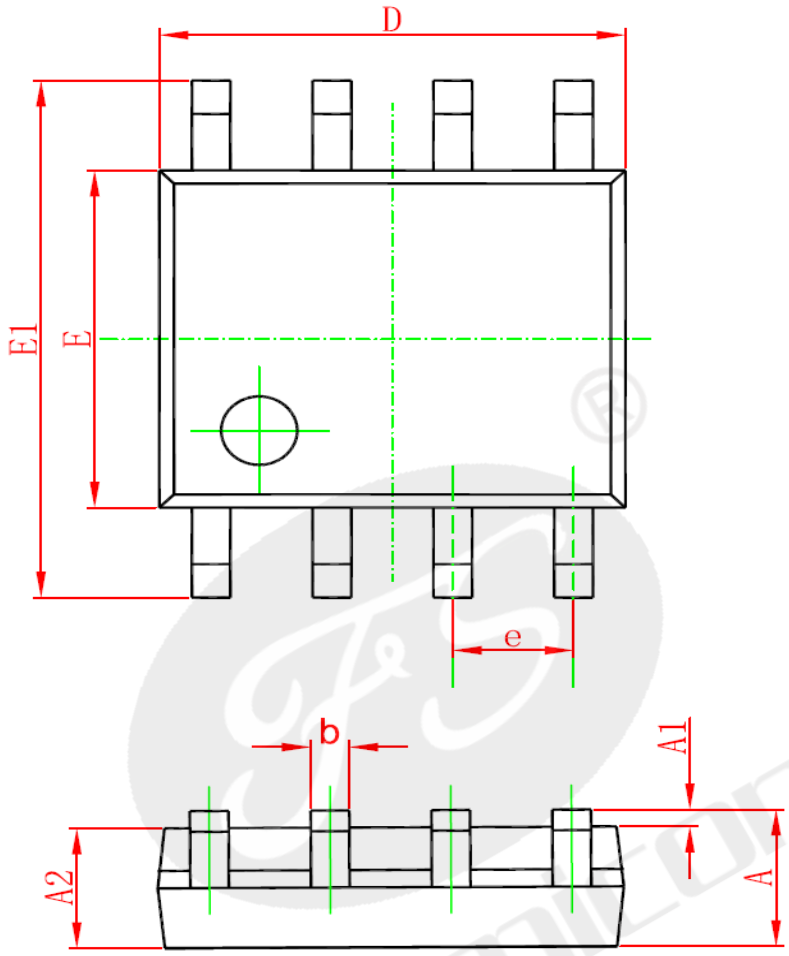


Figure 14. Typical Gate Charge vs Gate-to-Source Voltage



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2021.05.01	1.0	Initial release	