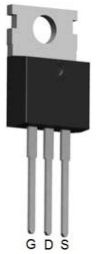
General Description

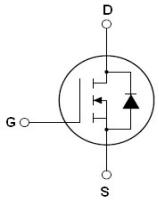
The FIR96N08PG is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged E_{AS} capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.



To-220 Top View

Features

- V_{DS}=80V; I_D=96A@ V_{GS}=10V; $R_{DS(ON)}$<7.2mΩ @ V_{GS}=10V
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

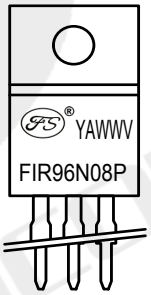


Schematic Diagram

Application

- 64V E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
V =Versio
FIR96N08P = Specific Device Code

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	80	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
$I_{D\ (DC)}$	Drain Current (DC) at Tc=25℃	96	A
$I_{D\ (DC)}$	Drain Current (DC) at Tc=100℃	67	A
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed **(Note 1)**	368	A
dv/dt	Peak Diode Recovery Voltage	7.3	V/ns
P_D	Maximum Power Dissipation(Tc=25℃)	146	W
	Derating Factor	0.93	W/℃
E_{AS}	Single Pulse Avalanche Energy **(Note 2)**	625	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature
2.E_{AS} condition:T_J=25℃,V_{DD}=40V,V_G=10V,R_G=25Ω

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	---	1.02	℃/W

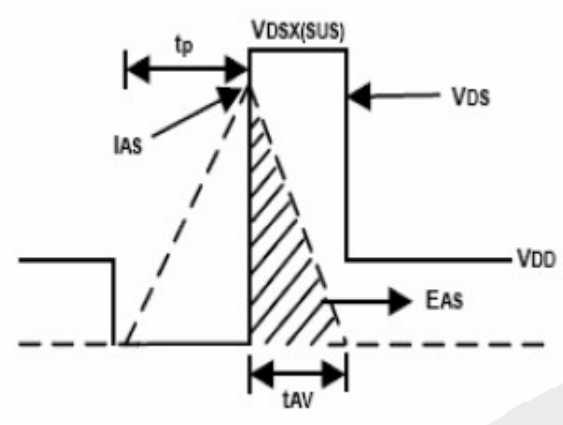
Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

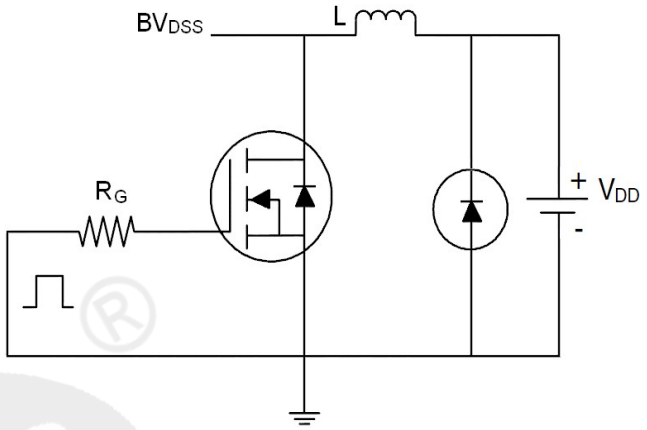
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	80			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=80V,V_{GS}=0V			1	μA
I_{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=80V,V_{GS}=0V			10	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2		4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=40A		6.2	7.2	mΩ
Dynamic Characteristics						
g_{FS}	Forward Transconductance	V_{DS}=10V,I_D=15A	20			S
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, f=1.0MHz		6396		PF
C_{oss}	Output Capacitance			387		PF
C_{rss}	Reverse Transfer Capacitance			256		PF
Q_g	Total Gate Charge	V_{DS}=50V,I_D=40A, V_{GS}=10V		117		nC
Q_{gs}	Gate-Source Charge			28		nC
Q_{gd}	Gate-Drain Charge			40		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V,I_D=40A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω		23		nS
t_r	Turn-on Rise Time			51		nS
$t_{d(off)}$	Turn-Off Delay Time			66		nS
t_f	Turn-Off Fall Time			23		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-drain Current(Body Diode)			96		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			372		A
V_{SD}	Forward On Voltage **(Note 1)**	T_J=25℃,I_{SD}=40A,V_{GS}=0V		0.89	0.99	V
t_{rr}	Reverse Recovery Time **(Note 1)**	T_J=25℃,I_F=75A di/dt=100A/μs		41		nS
Q_{rr}	Reverse Recovery Charge **(Note 1)**			86		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

Notes 1.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting T_J=25℃

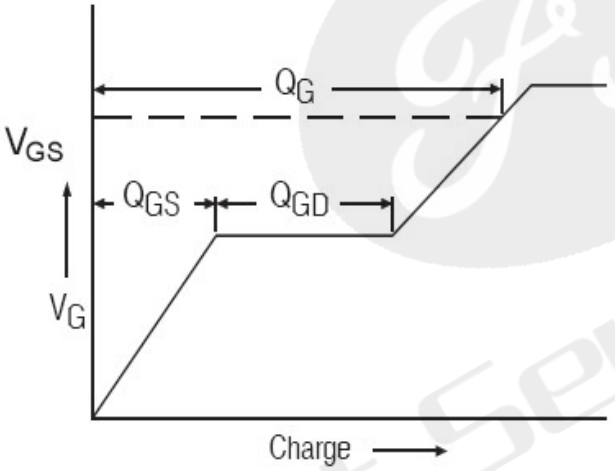
Test Circuit

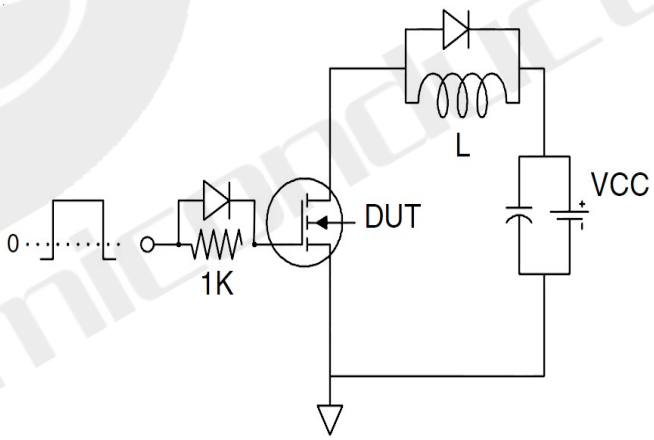
1) E_{AS} Test Circuits



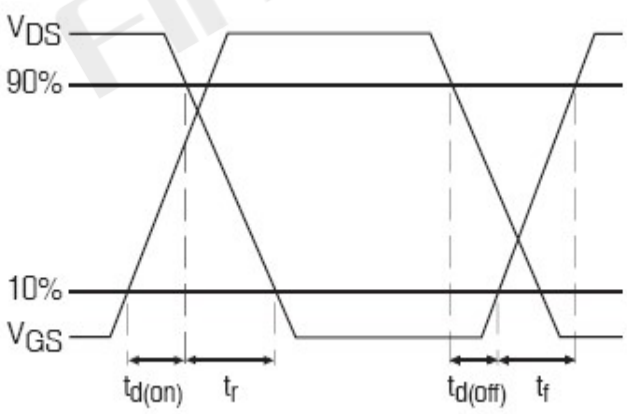


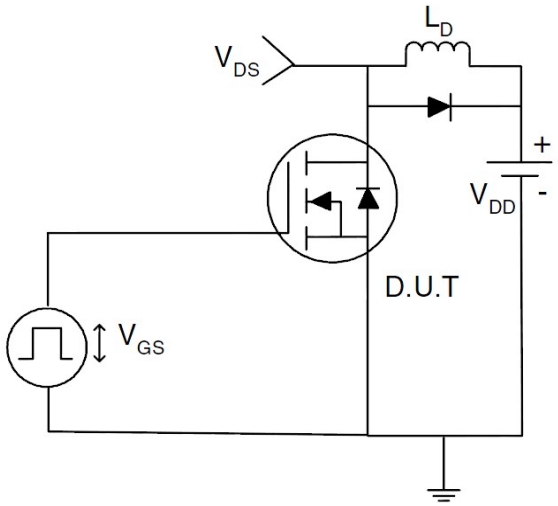
2) Gate Charge Test Circuit:





3) Switch Time Test Circuit:





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

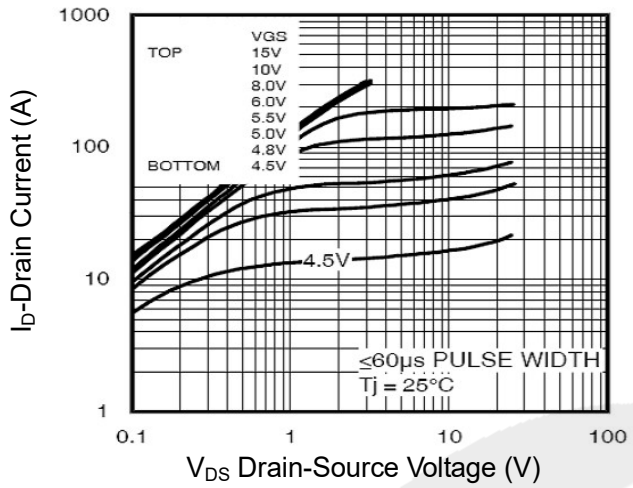


Figure2. Transfer Characteristics

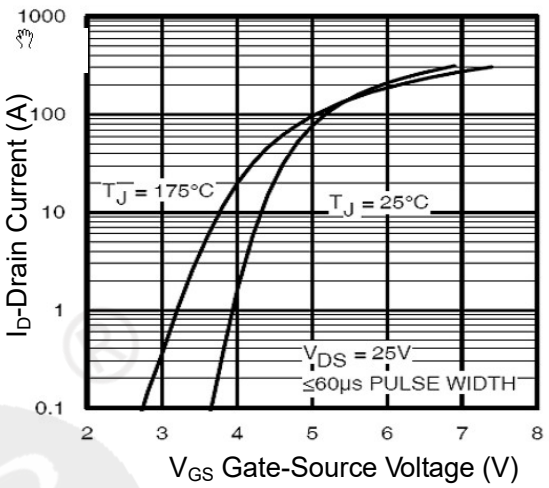


Figure3. BVDSS vs Junction Temperature

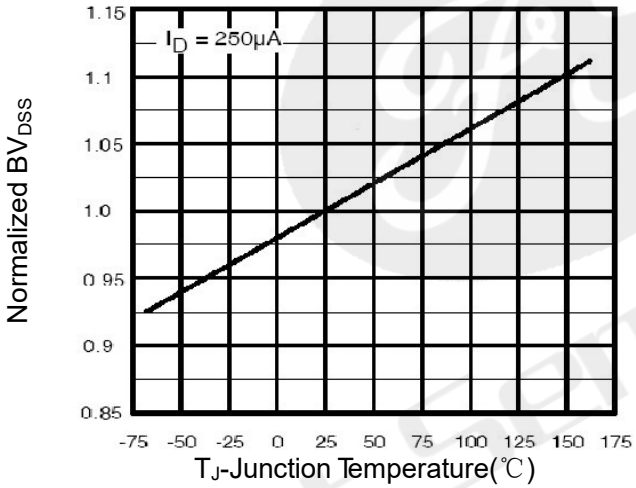


Figure4. ID vs Junction Temperature

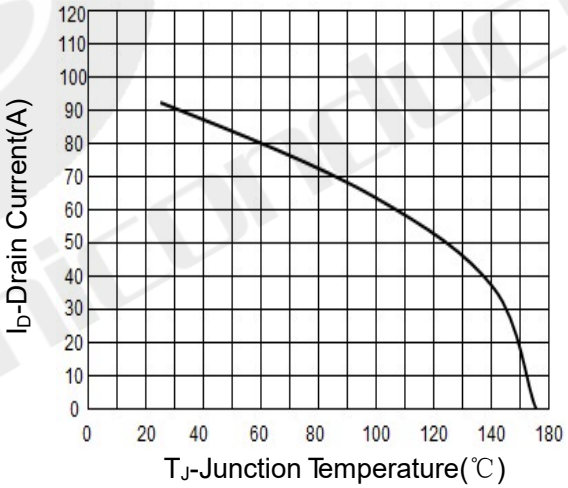


Figure5. VGS(th) vs Junction Temperature

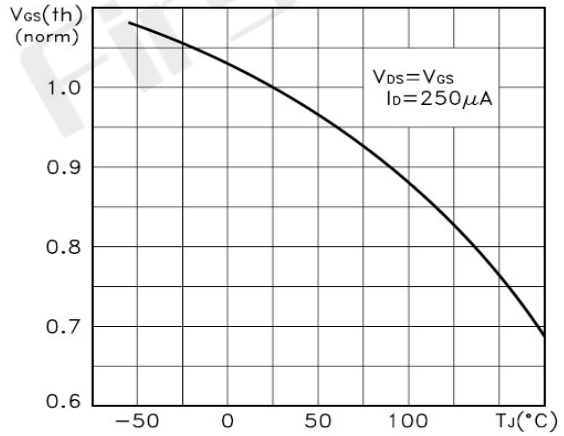
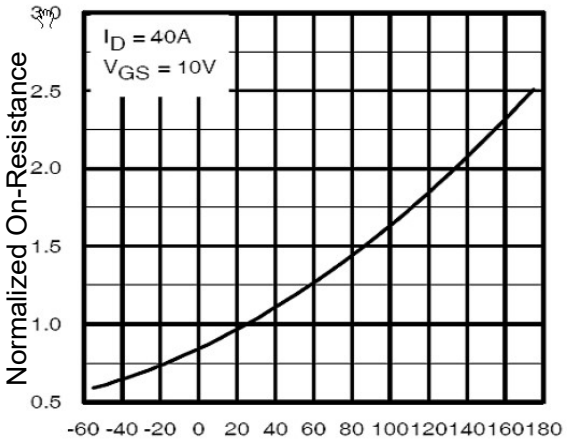


Figure6. Rdson Vs Junction Temperature



TJ-Junction Temperature(℃)

Figure7. Gate Charge

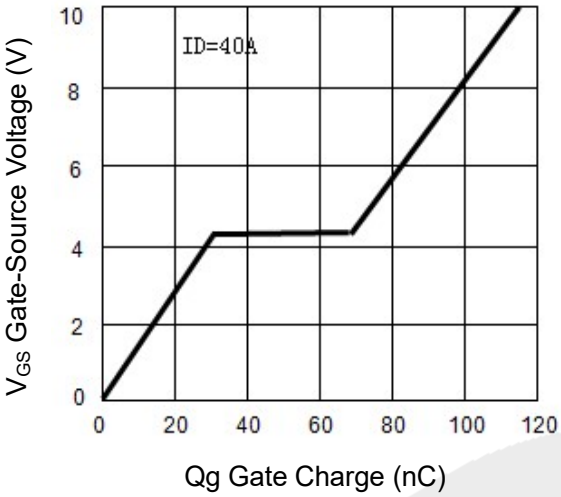


Figure8. Capacitance vs Vds

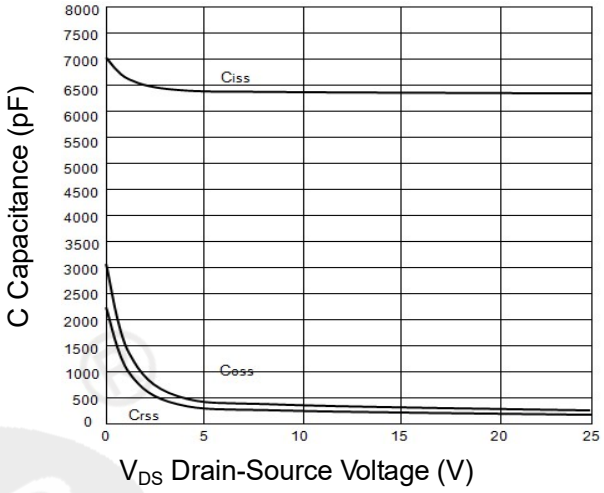


Figure9. Source- Drain Diode Forward

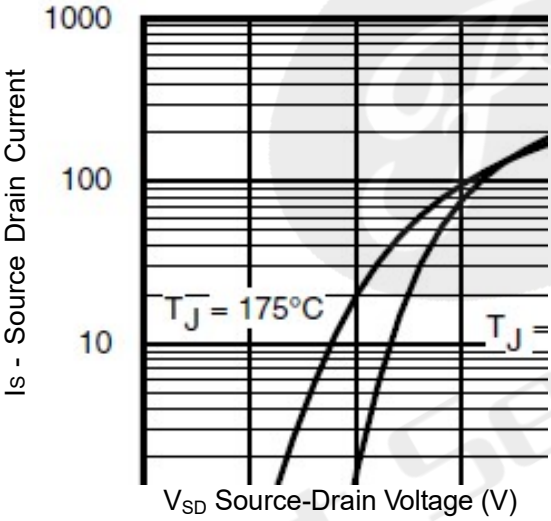


Figure10. Safe Operation Area

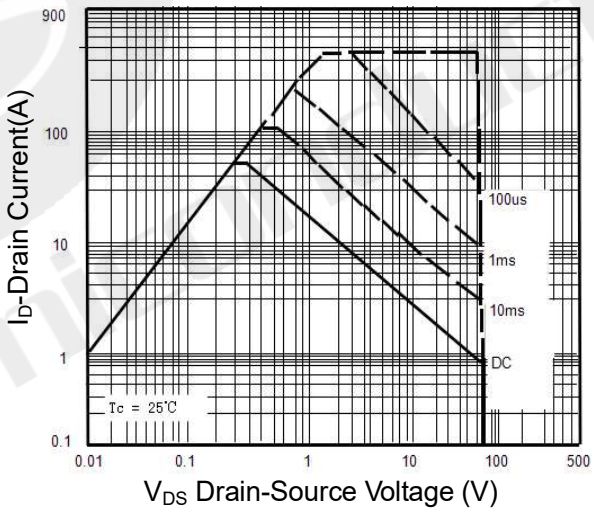
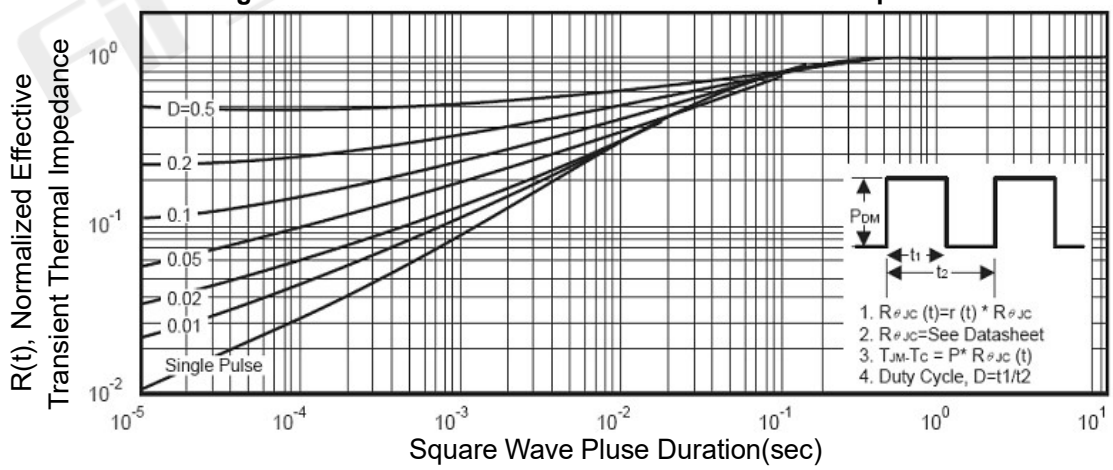


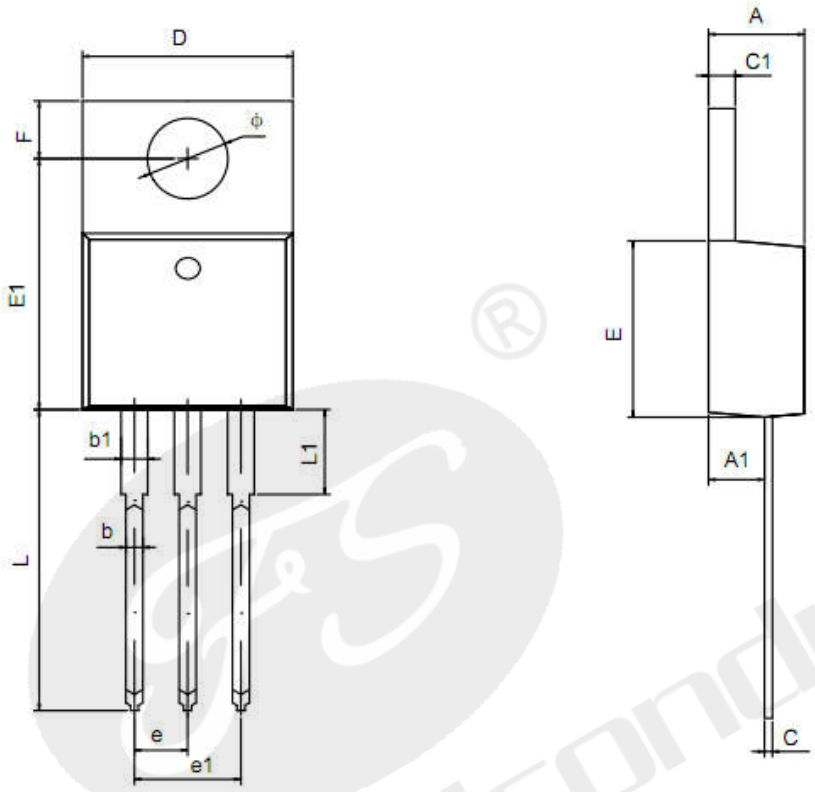
Figure11. Normalized Maximum Transient Thermal Impedance



Package Dimensions

TO-220

Units: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.42	4.72	0.174	0.188
A1	2.52	2.82	0.099	0.111
b	0.71	0.91	0.028	0.036
b1	1.17	1.37	0.046	0.054
c	0.36	0.46	0.014	0.018
c1	1.17	1.37	0.046	0.054
D	9.95	10.25	0.392	0.0404
E	8.8	9.1	0.346	0.358
E1	12.55	12.85	0.494	0.506
e	2.540TYP		0.100TYP	
e1	4.98	5.18	0.196	0.204
F	2.59	2.89	0.102	0.114
L	13.08	13.48	0.515	0.531
L1	3.4	3.6	0.134	0.142
Φ	3.8	3.95	0.15	0.156

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2021.09.01	1.0	Initial release	