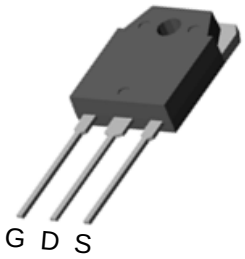
First Semiconductor

FIR24N50APTG

High Voltage N-Channel MOSFET

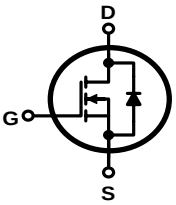
PIN Connection TO-3P



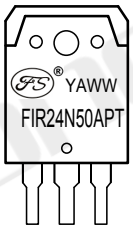
Features

- Low Intrinsic Capacitances
- Excellent Switching Characteristics
- Extended Safe Operating Area
- Unrivalled Gate Charge :90 nC (Typ.)
- BVDSS=500V,ID=24A
- Lower $R_{DS(on)}$: 0.2 Ω (Max) @VG=10V
- 100% Avalanche Tested

Schematic diagram



Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
FIR24N50APT= Specific Device Code

Absolute Maximum Ratings Tc=25℃ unless other wise noted

Symbol	Parameter	FIR24N50ANG	Units
V_{DSS}	Drain-Sourse Voltage	500	V
I_D	Drain Current -continuous (Tc=25℃)	24	A
	-continuous (Tc=100℃)	15.2	A
V_{GS}	Gate-Sourse Voltage	±30	V
E_{AS}	Single Plused Avanche Energy (Note1)	1100	mJ
I_{AR}	Avalanche Current (Note2)	24	A
P_D	Power Dissipation (Tc=25℃)	290	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 ~ +150	℃
TL	Maximum lead temperature for soldering purpose,1/8" from case for 5 seconds	300	℃

Thermal Characteristics

Symbol	Parameter	Typ.	Max	Units
$R_{\theta JC}$	Thermal Resistance,Junction to Case	--	0.43	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient	--	62.5	℃/W

Electrical Characteristics Tc=25℃ unless other wise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourse Breakdown Voltage	ID=250μA，VGS=0	500	--	--	V
$\triangle BV_{DSS}/\triangle T_J$	Breakdown Voltage Temperature Conficient	I_D=250μA,Reference to 25℃	--	0.53	--	V/℃
IDSS	Zero Gate Voltage Drain Current	Vds=500V, Vgs=0V	--	--	1	μA
		Vds=400V, Tc=125℃			10	μA
IGSSF	Gate-body leakage Current, Forward	Vgs=+30V, Vds=0V	--	--	100	nA
IGSSR	Gate-body leakage Current, Reverse	Vgs=-30V, Vds=0V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Date Threshold Voltage	Id=250uA,Vds=Vgs	2	--	4	V
$R_{DS(on)}$	Static Drain-Sourse On-Resistance	Id=10A,Vgs=10V	--	--	0.3	Ω
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=25V，VGS=0，f=1.0MHz	--	3500	4500	pF
Coss	Output Capacitance		--	520	670	pF
Crss	Reverse Transfer Capacitance		--	55	70	pF
Switching Characteristics						
Td(on)	Turn-On Delay Time	VDD=250V，ID=24A，RG=25Ω (Note 3,4)	--	80	170	nS
Tr	Turn-On Rise Time		--	250	500	nS
Td(off)	Turn-Off Delay Time		--	200	400	nS
Tf	Turn-Off Fall Time		--	155	320	nS
Qg	Total Gate Charge	VDS=400,VGS=10V，ID=24A (Note 3,4)	--	90	120	nC
Qgs	Gate-Sourse Charge		--	23	--	nC
Qgd	Gate-Drain Charge			44	--	nC
Drain-Sourse Diode Characteristics and Maximum Ratings						
I_S	Maximun Continuous Drain-Sourse Diode Forward Current		--	--	24	A
I_{SM}	Maximun Plused Drain-Sourse DiodeForwad Current		--	--	96	A
V_{SD}	Drain-Sourse Diode Forward Voltage	Id=24A	--	--	1.4	V
trr	Reverse Recovery Time	I_S=24A,V_{GS} =0V di$_F$/dt=100A/μs (Note3)	--	400	--	nS
Qrr	Reverse Recovery Charge		--	4.3	--	μC

*Notes 1, L=3.4mH, IAS=24.0A, VDD=50V, RG=25Ω, Starting TJ =25°C

2, Repetitive Rating : Pulse width limited by maximum junction temperature

3, Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

4, Essentially Independent of Operating Temperature

Typical Characteristics

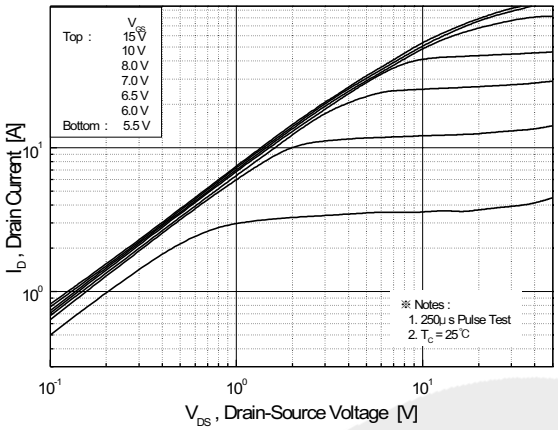


Figure 1. On-Region Characteristics

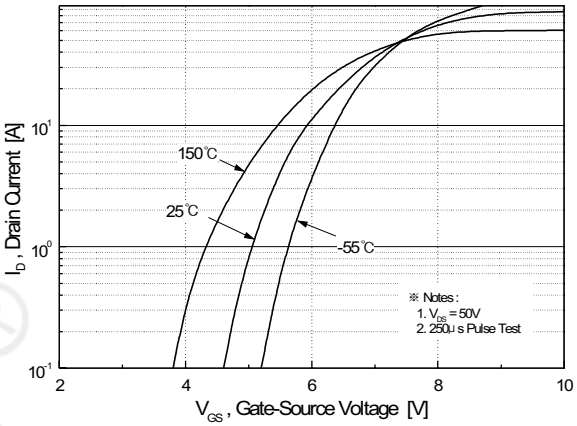


Figure 2. Transfer Characteristics

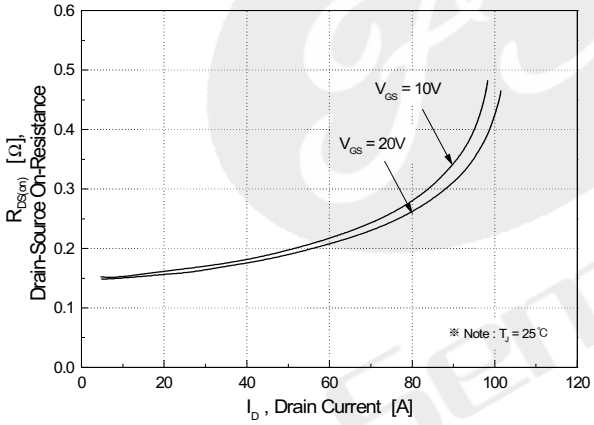


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

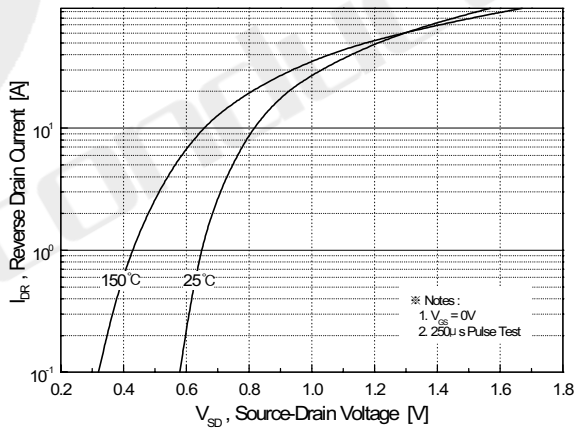


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

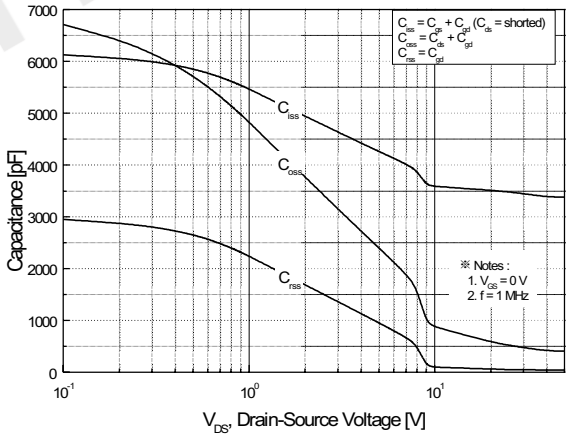


Figure 5. Capacitance Characteristics

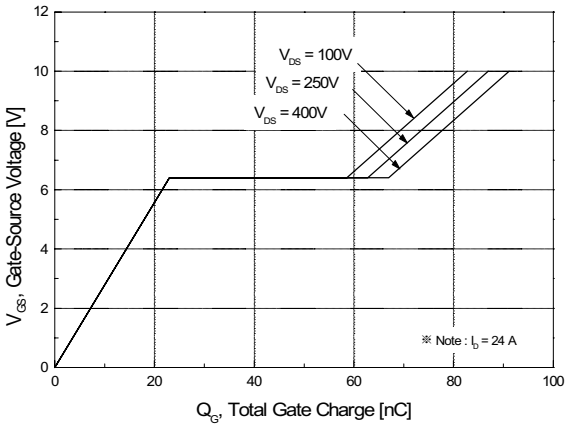


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

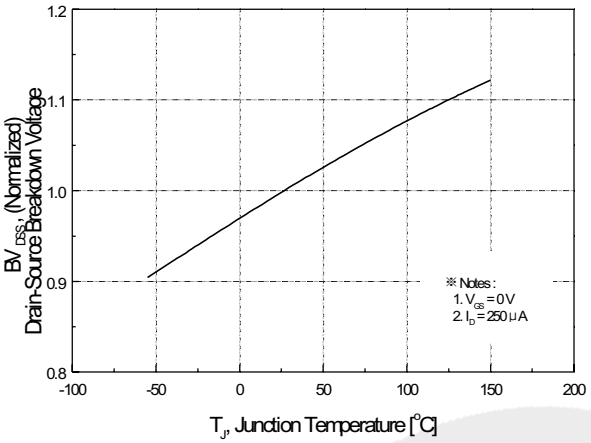


Figure 7. Breakdown Voltage Variation vs. Temperature

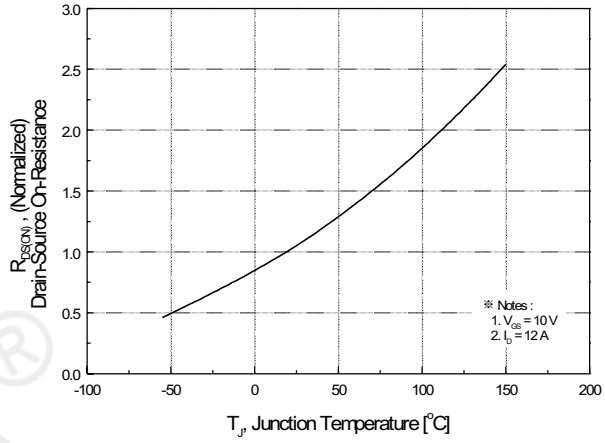


Figure 8. On-Resistance Variation vs. Temperature

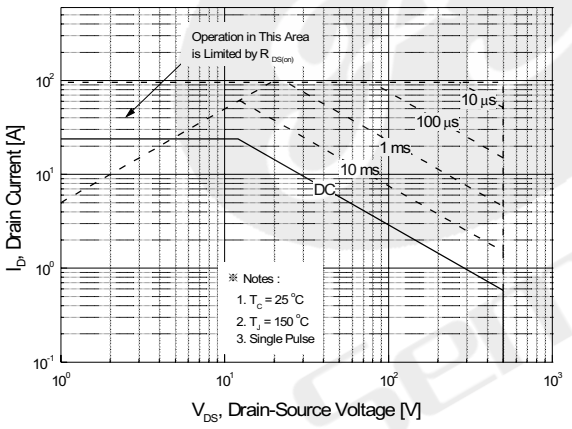


Figure 9. Maximum Safe Operating Area

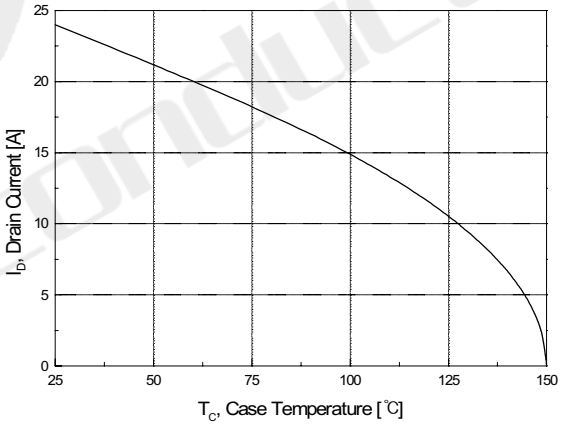


Figure 10. Maximum Drain Current vs. Case Temperature

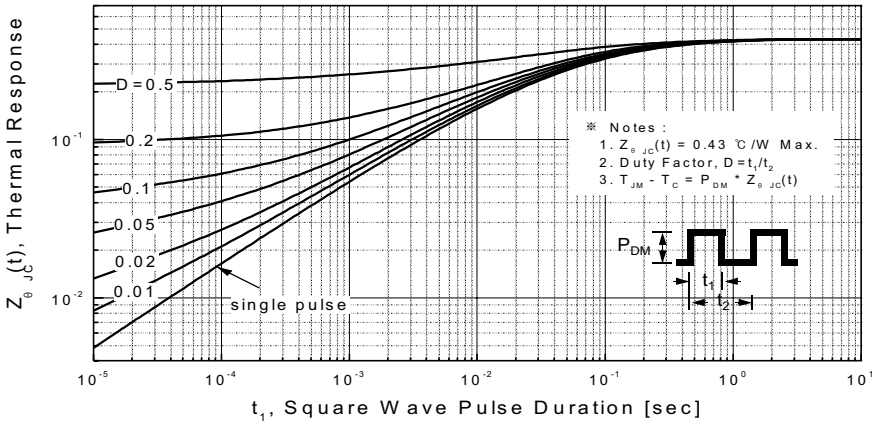
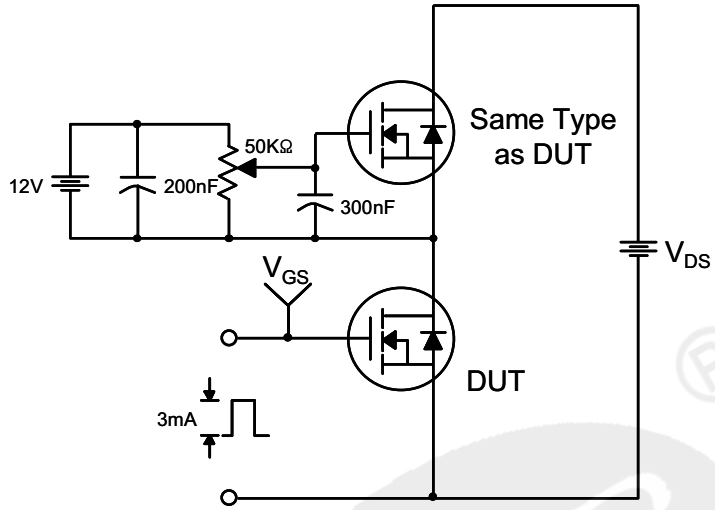
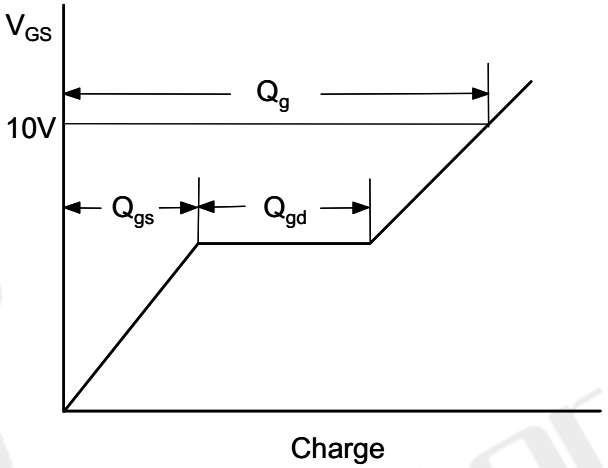


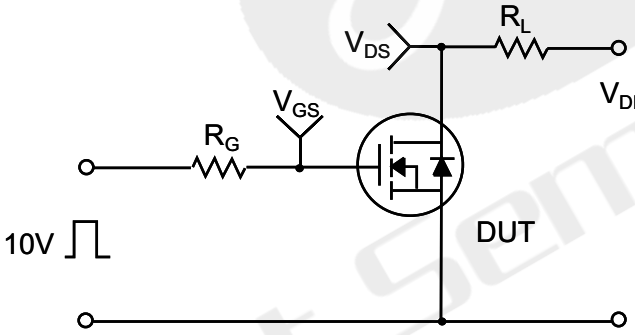
Figure 11. Transient Thermal Response Curve

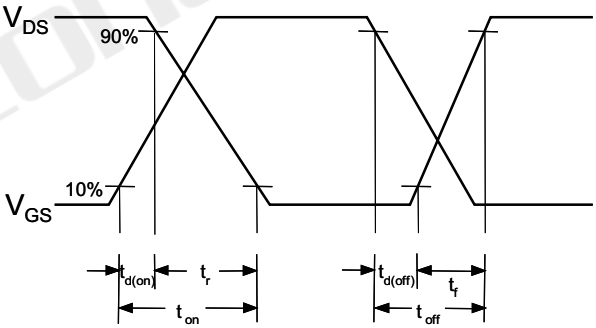
Gate Charge Test Circuit & Waveform

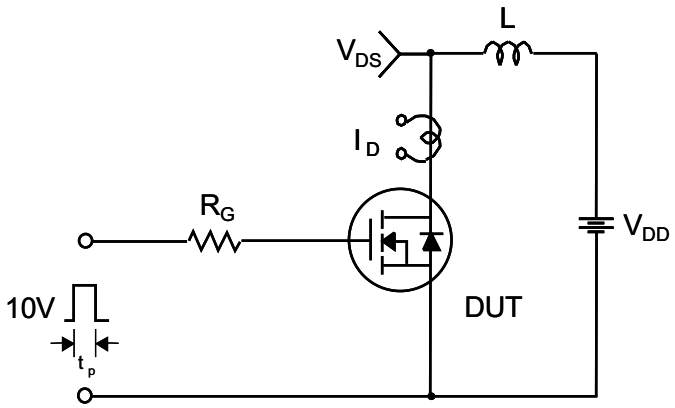




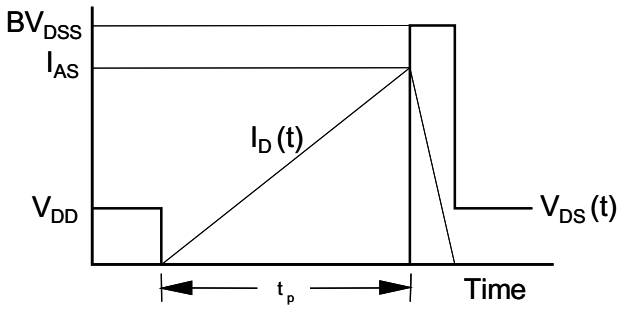
Resistive Switching Test Circuit & Waveforms



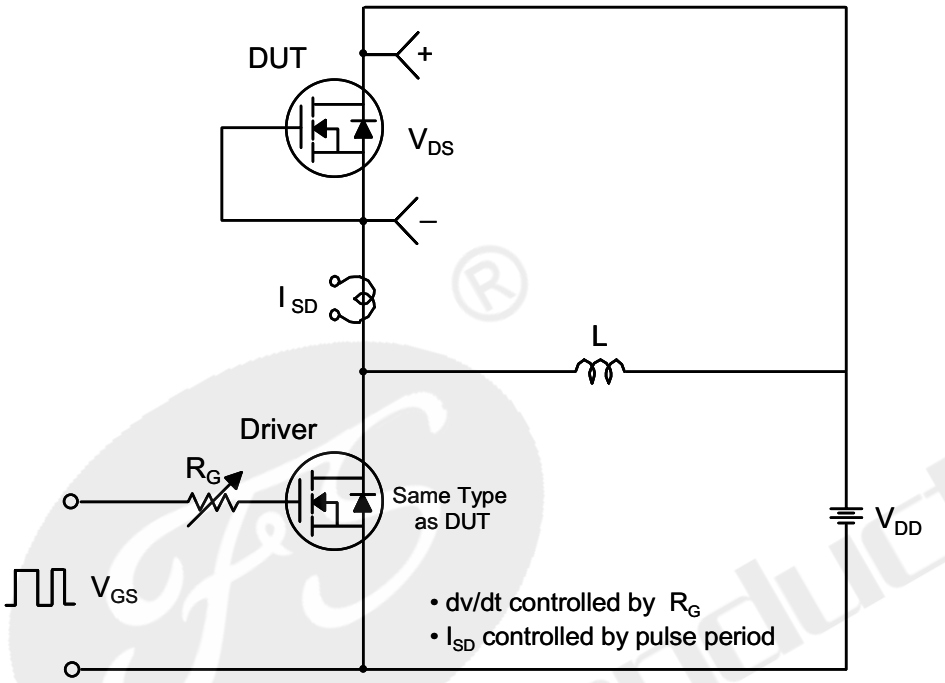


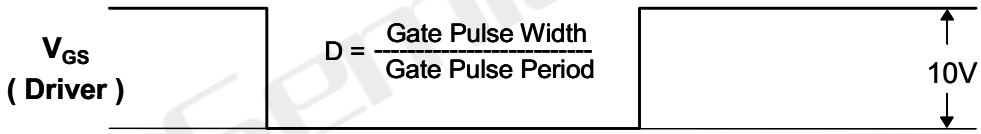


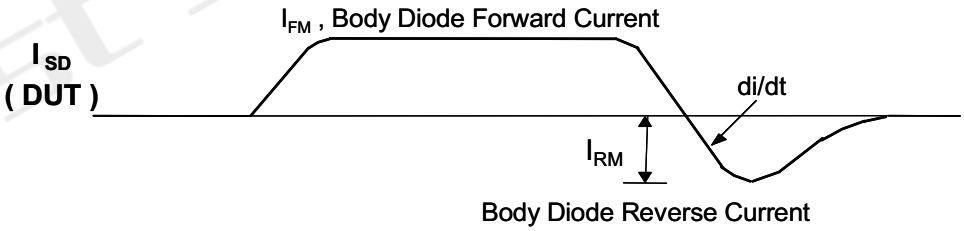
$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

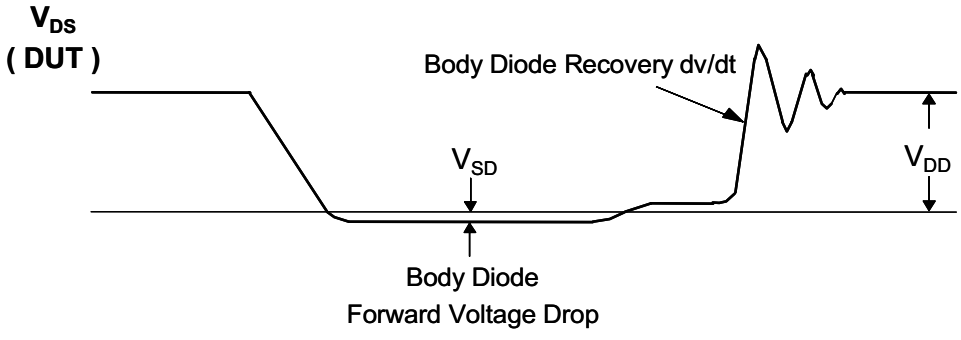


Peak Diode Recovery dv/dt Test Circuit & Waveforms





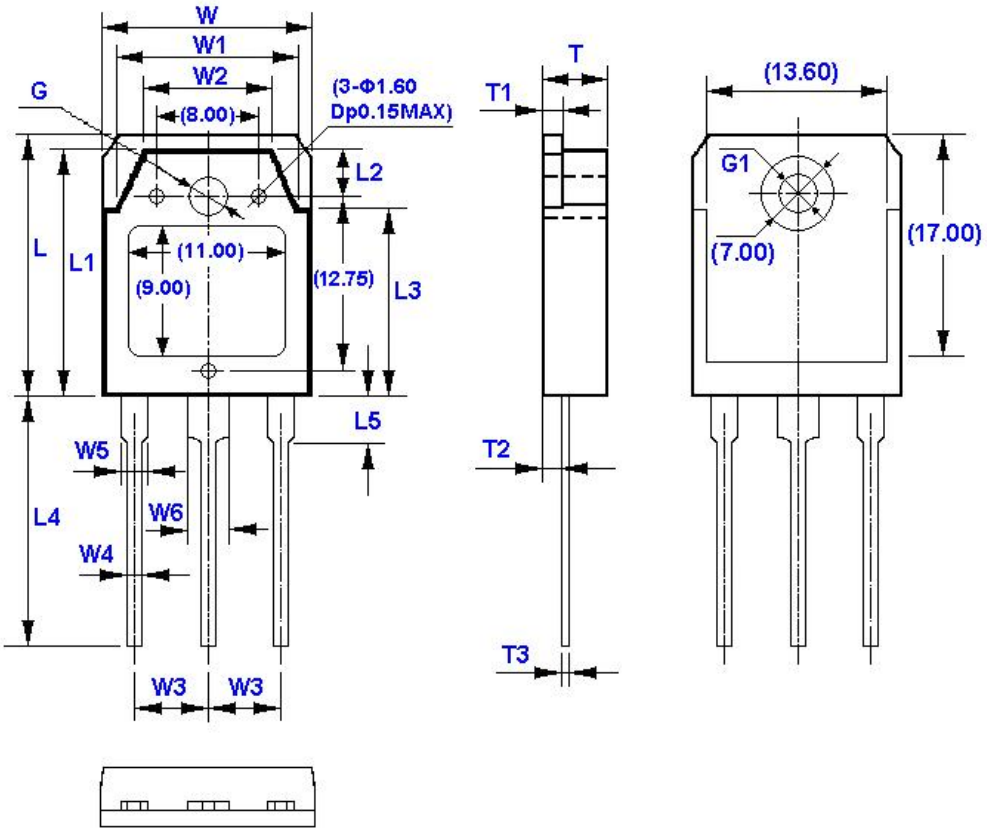




Package Outline Dimensions

TO-3P

Units: mm



符号	尺寸		符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max		Min	Max
W	15.40	15.80	W5	1.80	2.20	L3	13.70	14.10	T2	1.20	1.60
W1	13.40	13.80	W6	2.80	3.20	L4	19.70	20.30	T3	0.55	0.75
W2	9.40	9.80	L	19.70	20.10	L5	3.30	3.70	G (Φ) (正面)	3.30	3.50
W3	5.45 (TYP)		L1	18.50	18.90	T	4.60	5.00	G1(Φ) (背面)	3.10	3.30
W4	0.80	1.20	L2	3.60	4.00	T1	1.45	1.65			

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	