



General Description

The FIR15N10LG is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

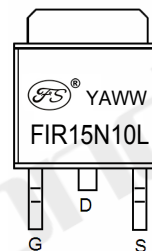
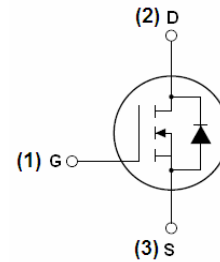
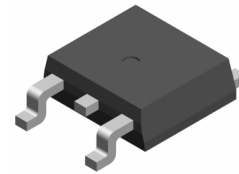
General Features

- $R_{DS(ON)} \leq 100m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

Application

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN Connection TO-252



Marking Diagram

- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR15N10L = Specific Device Code

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Tj=150°C)	I_D	Tc=25°C	15
		Tc=70°C	12
Pulsed Drain Current	I_{DM}	59	A
Maximum Power Dissipation	P_D	Tc=25°C	35
		Tc=70°C	22
Operating Junction Temperature	T_J	-55 to 150	°C
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	3.57	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper

**Absolute Maximum Ratings** ($T_A=25^{\circ}\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 20	V

Electrical Characteristics ($T_j=25^{\circ}\text{C}$ Unless Otherwise Specified)

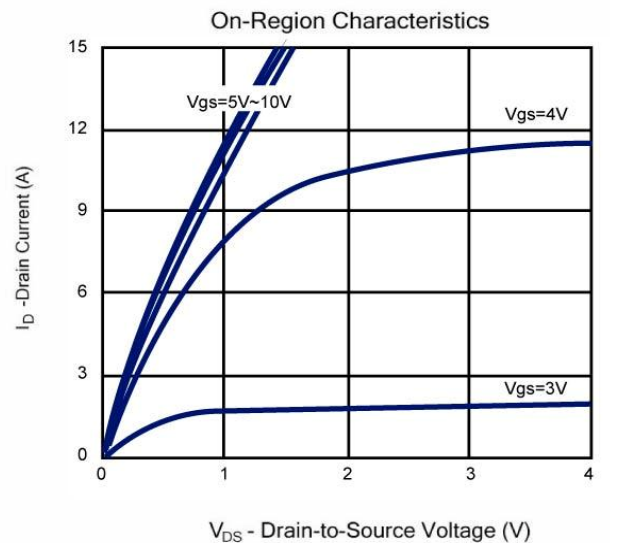
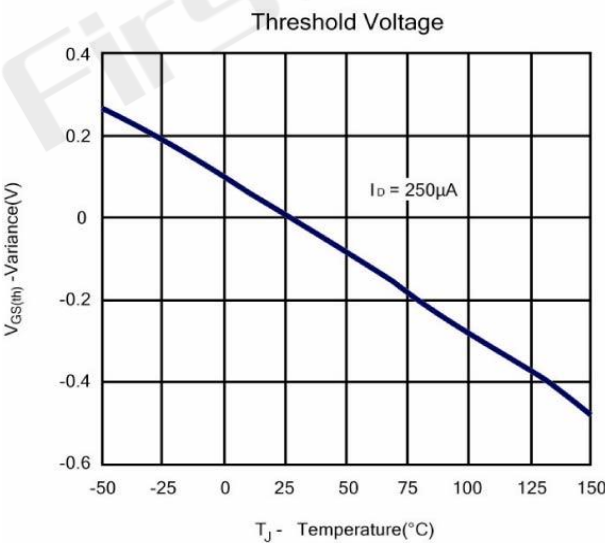
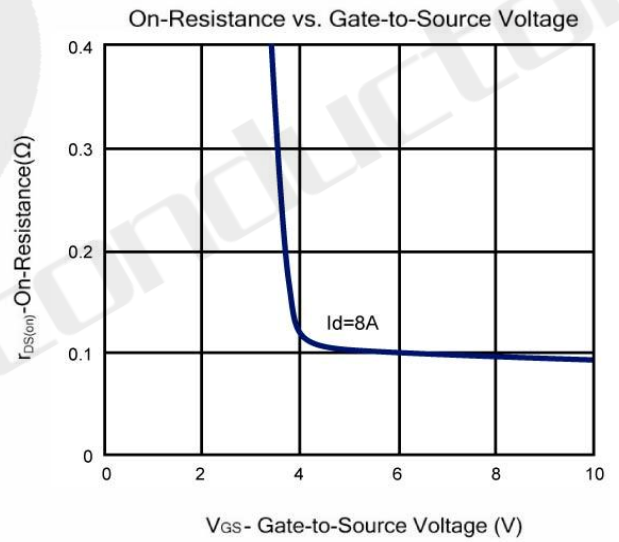
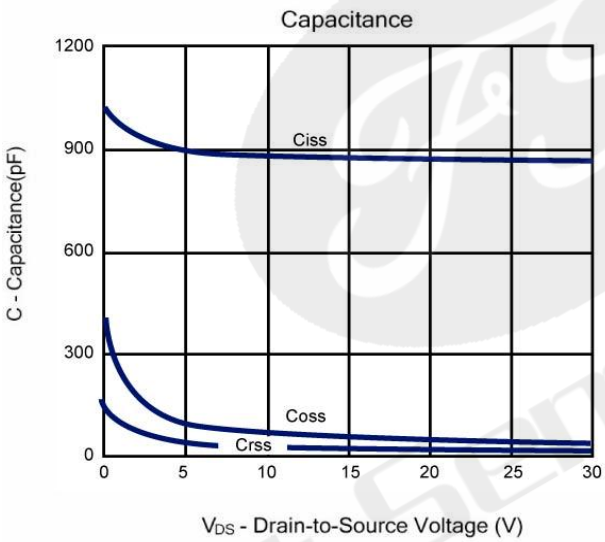
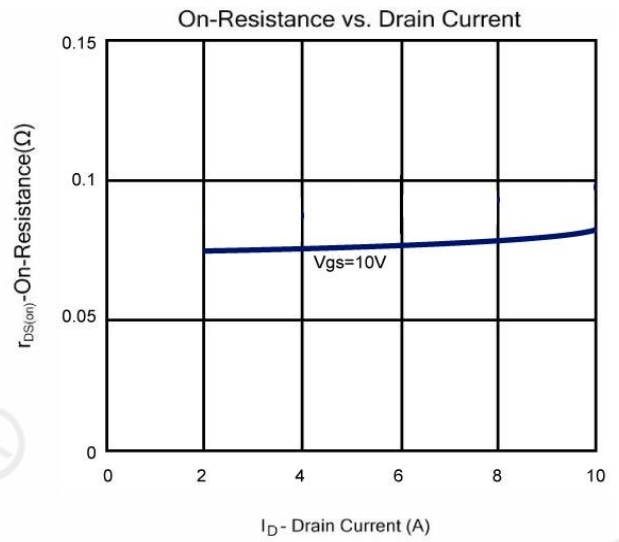
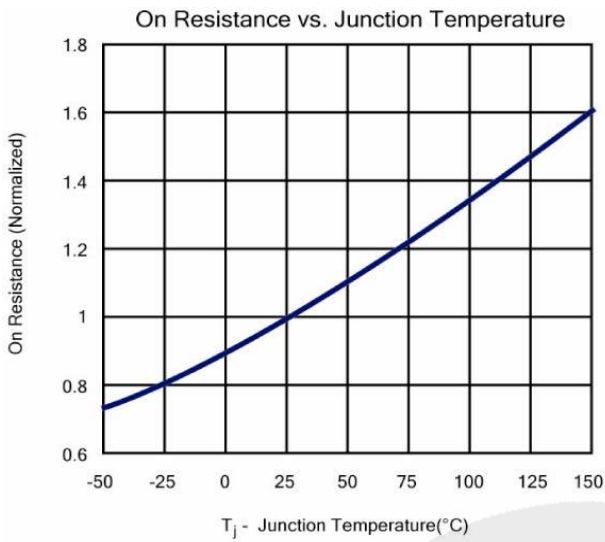
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0, I_D=250 \mu\text{A}$	100			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250 \mu\text{A}$	1		3	V
I_{GSS}	Gate Body Leakage	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=8\text{A}$		80	100	$\text{m}\Omega$
V_{SD}	Diode Forward Voltage	$I_S=8\text{A}, V_{GS}=0\text{V}$		1		V
DYNAMIC						
Q_g	Total Gate Charge(10V)	$V_{DS}=80\text{V}, V_{GS}=4.8\text{V}, I_D=10\text{A}$		22		nC
Q_g	Total Gate Charge(4.8V)			10		
Q_{gs}	Gate-Source Charge			4		
Q_{gd}	Gate-Drain Charge			7		
C_{iss}	Input capacitance	$V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		700		pF
C_{oss}	Output Capacitance			70		
C_{rss}	Reverse Transfer Capacitance			50		
R_g	Gate Resistance	$V_{DS}=0\text{V}, V_{GS}=25\text{V}, f=1\text{MHz}$		2		Ω
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=50\text{V}, R_L=5\Omega, V_{GEN}=10\text{V}, R_G=1\Omega$		11		ns
t_r	Turn-On Rise Time			30		
$t_{d(off)}$	Turn-Off Delay Time			35		
t_f	Turn-Off Fall Time			3.5		

Notes: a. Based on epoxy or solder paste and bond wire Al wire 10mil \times 2(S), Au wire 1.5mil \times 1(G) on each die of TO-252-3L package.

b. Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

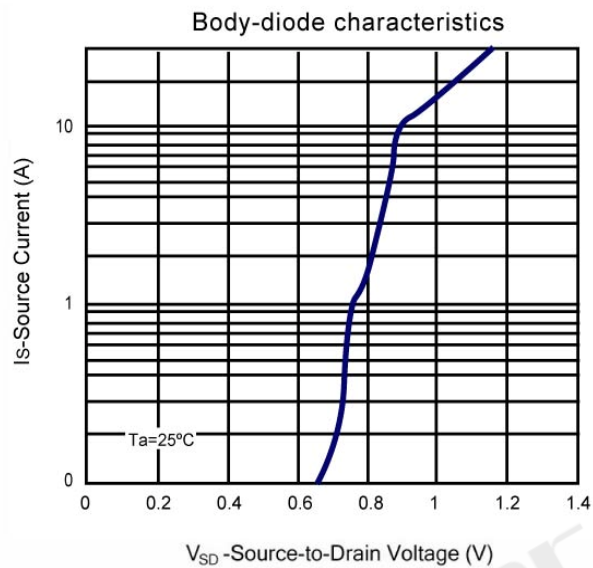
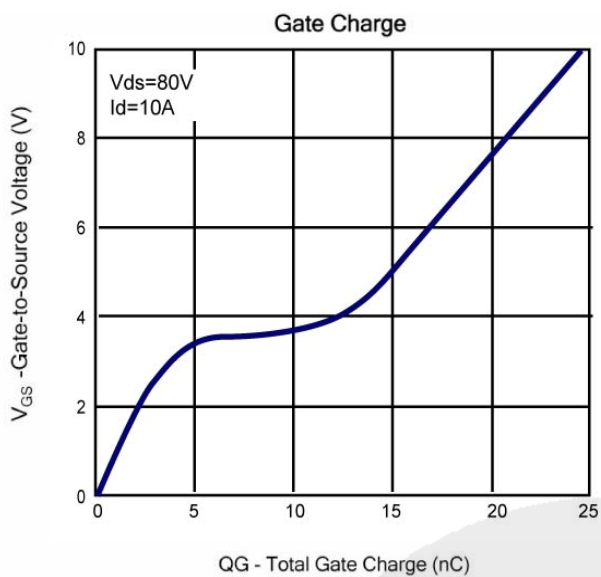


Typical Characteristics (T_J =25°C Noted)



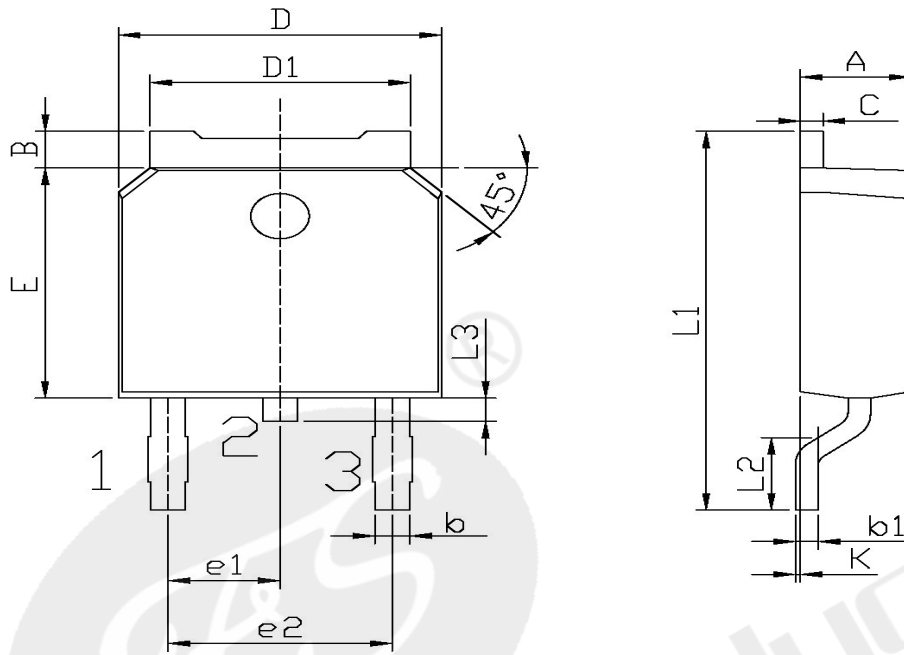


Typical Characteristics (T_J =25°C Noted)



Package Dimensions

TO-252



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	2.20	2.40	E	5.95	6.25
B	0.95	1.25	e1	2.24	2.34
b	0.70	0.90	e2	4.43	4.73
b1	0.45	0.55	L1	9.85	10.35
C	0.45	0.55	L2	1.25	1.75
D	6.45	6.75	L3	0.60	0.90
D1	5.20	5.40	K	0.00	0.10



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	