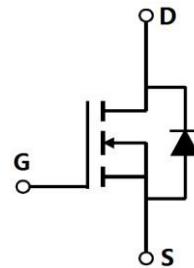


100V N-SGT Enhancement Mode MOSFET
General Description

12N10D use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in Synchronous-rectification applications.


Features

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery
- Invertors
- Synchronous-rectification applications

Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC
- Synchronous-rectification applications

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
12N10D	TO-252	12N10D	2500

Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	12	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D,\text{pulse}}$	21	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	17	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	1.2	mJ
Operation and storage temperature	T_{STG}, T_J	-55 to 150	$^\circ\text{C}$



100V N-SGT Enhancement Mode MOSFET
Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R _{θJC}	7.4	°C/W
Thermal resistance, junction-ambient ⁴⁾	R _{θJA}	62	°C/W

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV _{DSS}	100			V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	1.5		2.5	V	V _{DS} =V _{GS} , I _D =250 μA
Drain-source on-state resistance	R _{DSON}		110	140	mΩ	V _{GS} =10 V, I _D =5 A
Drain-source on-state resistance	R _{DSON}		160	300	mΩ	V _{GS} =4.5 V, I _D =3 A
Gate-source leakage current	I _{GSS}			100	nA	V _{GS} =20 V
				-100		V _{GS} =-20 V
Drain-source leakage current	I _{DSS}			1	uA	V _{DS} =100 V, V _{GS} =0 V
Input capacitance	C _{iss}		206.1		pF	V _{GS} =0 V, V _{DS} =50 V, f=100 kHz
Output capacitance	C _{oss}		28.9		pF	
Reverse transfer capacitance	C _{rss}		1.4		pF	
Turn-on delay time	t _{d(on)}		14.7		ns	V _{GS} =10 V, V _{DS} =50 V, R _G =2 Ω, I _D =5 A
Rise time	t _r		3.5		ns	
Turn-off delay time	t _{d(off)}		20.9		ns	
Fall time	t _f		2.7		ns	
Total gate charge	Q _g		4.3		nC	I _D =5 A, V _{DS} =50 V, V _{GS} =10 V
Gate-source charge	Q _{gs}		1.5		nC	
Gate-drain charge	Q _{gd}		1.1		nC	
Gate plateau voltage	V _{plateau}		5.0		V	
Diode forward current	I _S			7	A	

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Pulsed source current	I _{SP}			21		V _{GS} <V _{th}
Diode forward voltage	V _{SD}			1.0	V	I _S =7 A, V _{GS} =0 V
Reverse recovery time	t _{rr}		32.1		ns	
Reverse recovery charge	Q _{rr}		39.4		nC	
Peak reverse recovery current	I _{rrm}		2.1		A	I _S =5 A, di/dt=100 A/μs

■ Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
- 5) V_{DD}=50 V, R_G=50 Ω, L=0.3 mH, starting T_j=25 °C.

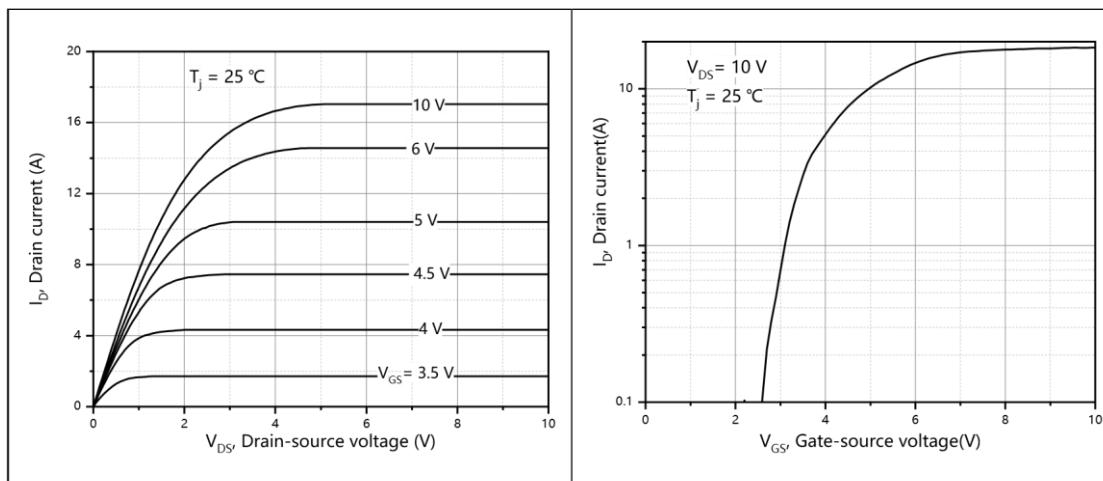
Electrical Characteristics Diagrams


Figure 1, Typ. output characteristics

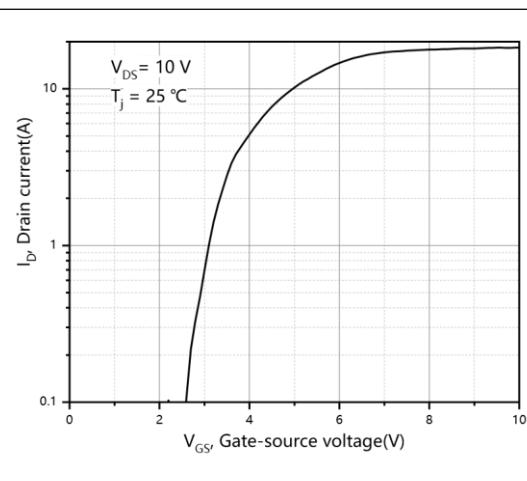


Figure 2, Typ. transfer characteristics

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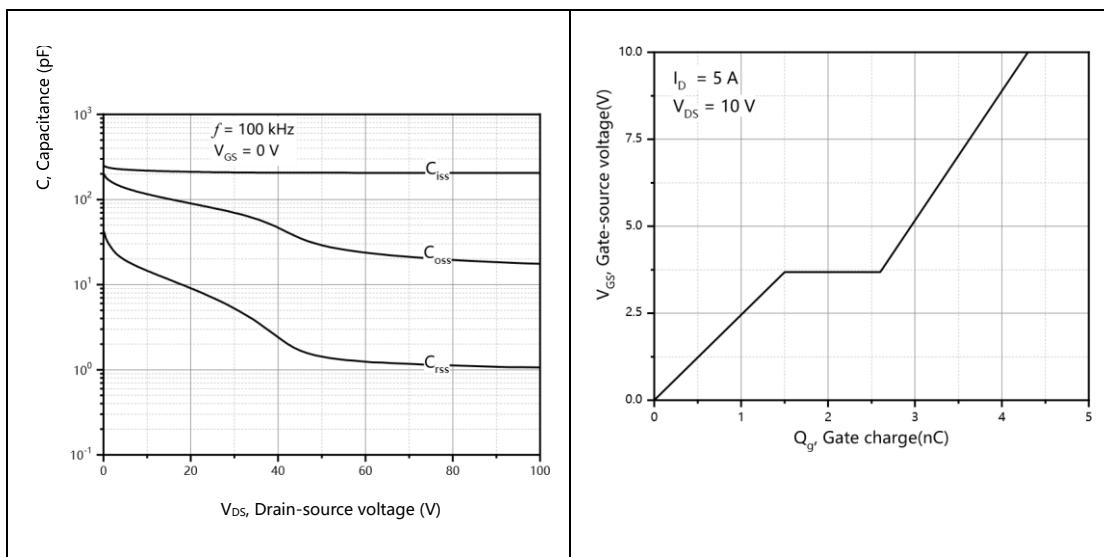


Figure 3, Typ. capacitances

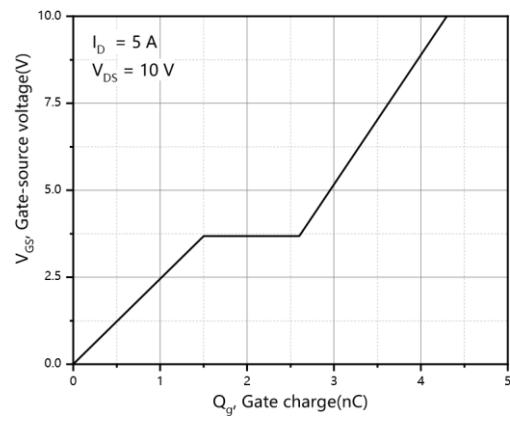


Figure 4, Typ. gate charge

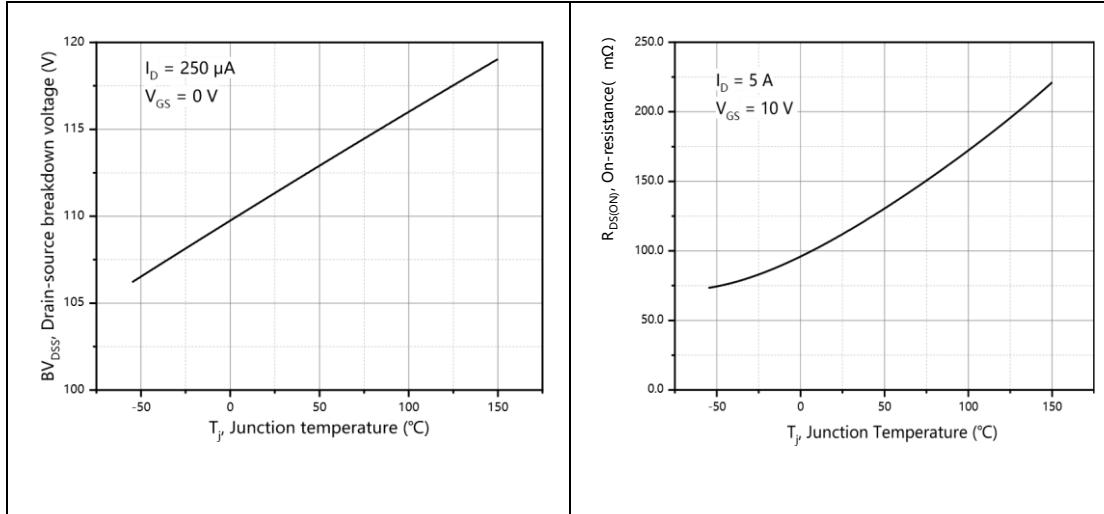


Figure 5, Drain-source breakdown voltage

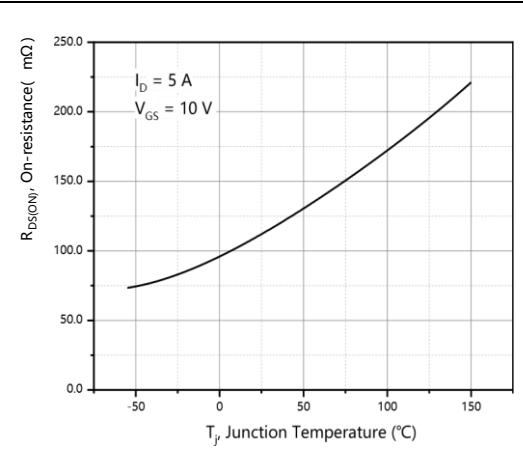


Figure 6, Drain-source on-state resistance

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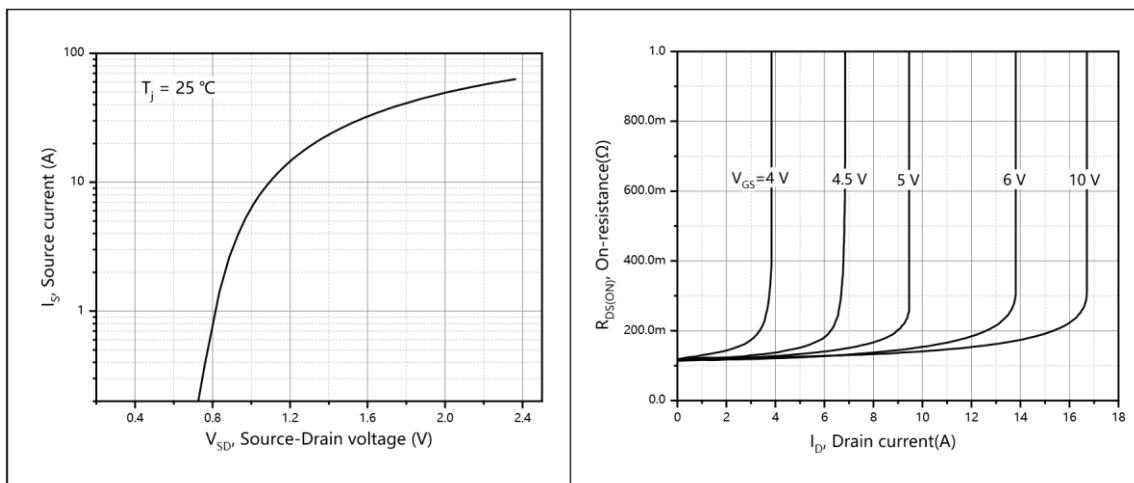


Figure 7, Forward characteristic of body diode

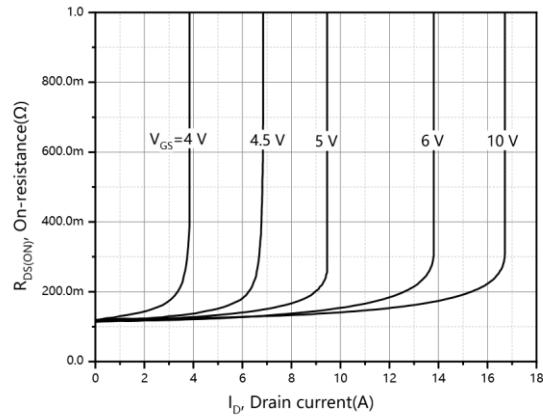


Figure 8, Drain-source on-state resistance

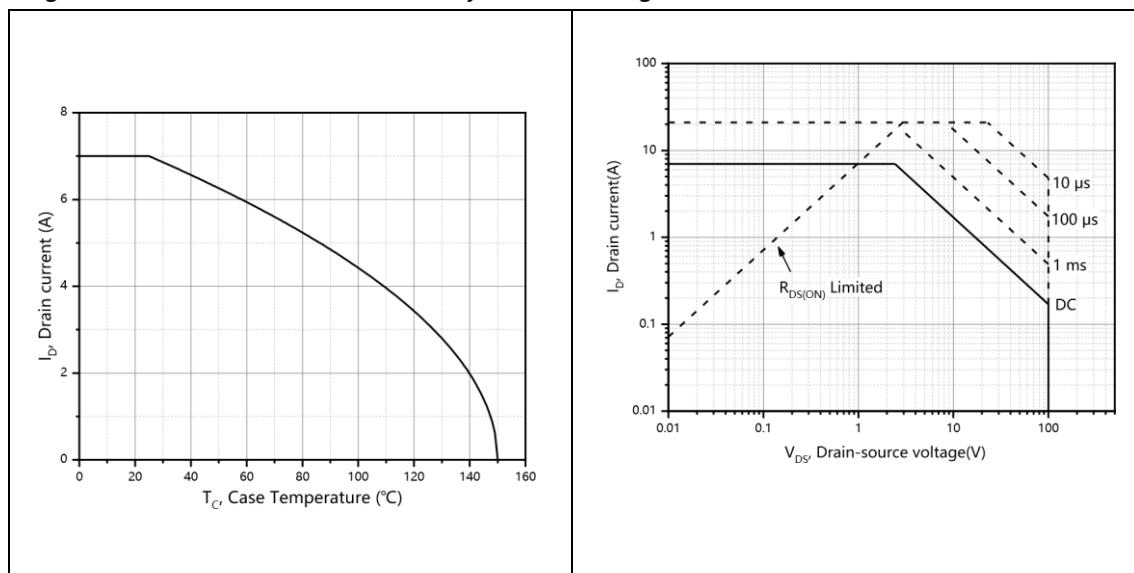


Figure 9, Drain current

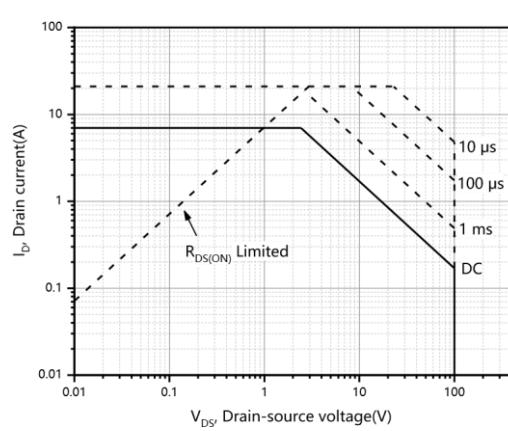
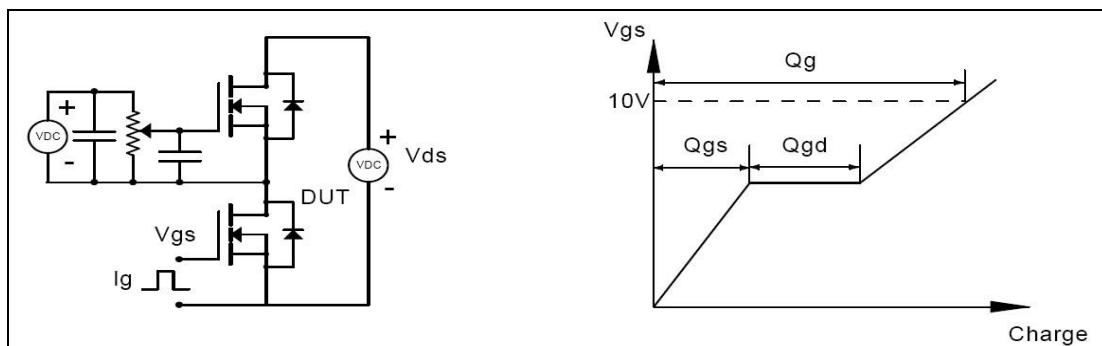
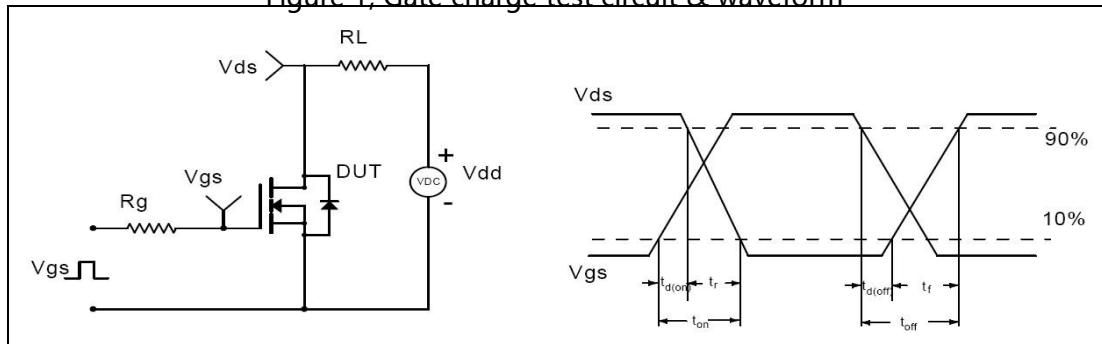
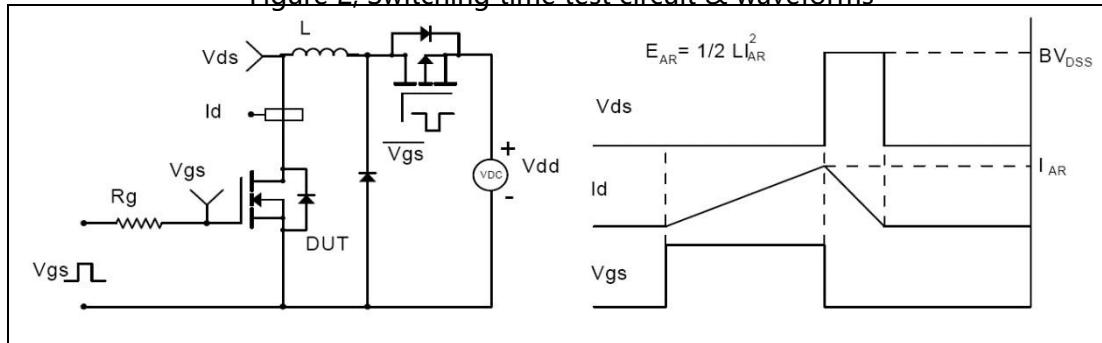
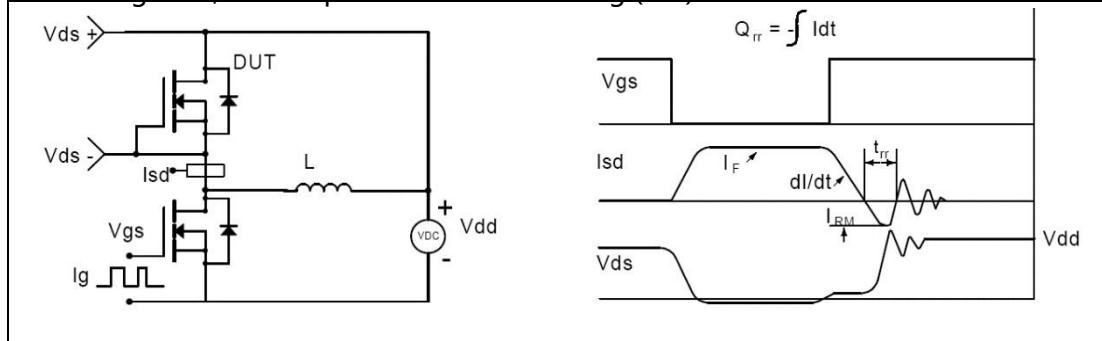
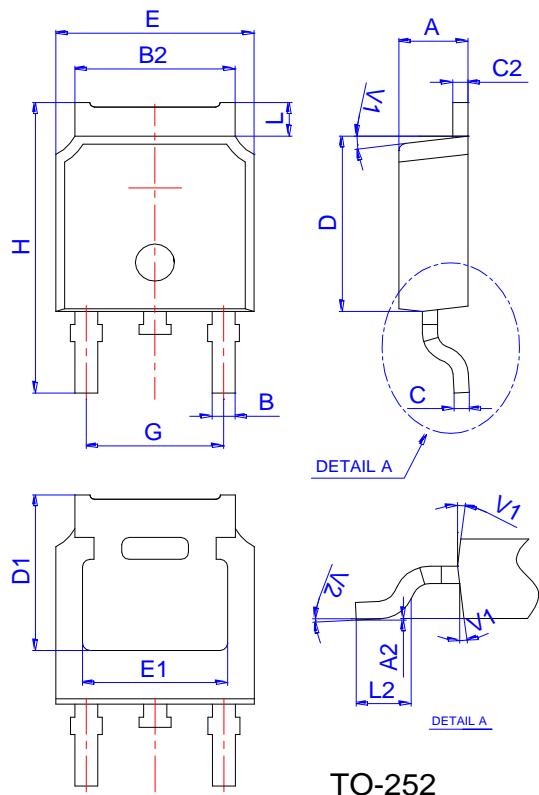
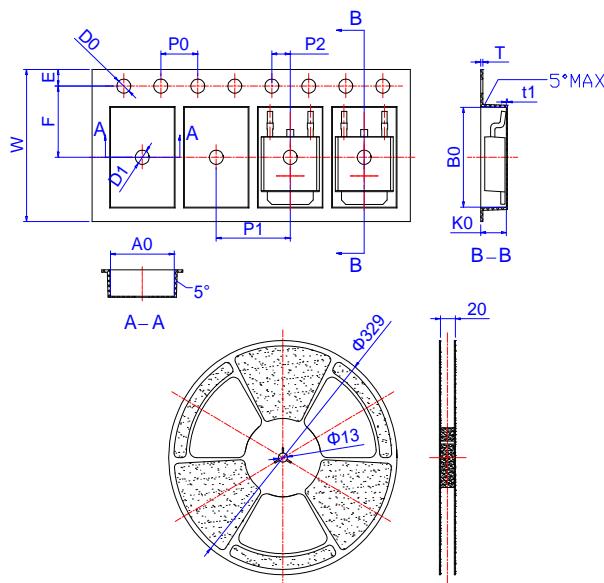


Figure 10, Safe operation area $T_C=25$ °C

100V N-SGT Enhancement Mode MOSFET
Test circuits and waveforms

Figure 1, Gate charge test circuit & waveform

Figure 2, Switching time test circuit & waveforms

Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

Figure 4, Diode reverse recovery test circuit & waveforms

100V N-SGT Enhancement Mode MOSFET
Package Mechanical Data


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10			2.50	0.083	
A2	0			0.10	0	0.004
B	0.66			0.86	0.026	0.034
B2	5.18			5.48	0.202	0.216
C	0.40			0.60	0.016	0.024
C2	0.44			0.58	0.017	0.023
D	5.90			6.30	0.232	0.248
D1	5.30REF			0.209REF		
E	6.40			6.80	0.252	
E1	4.63				0.182	
G	4.47			4.67	0.176	0.184
H	9.50			10.70	0.374	0.421
L	1.09			1.21	0.043	0.048
L2	1.35			1.65	0.053	0.065
V1		7°				7°
V2	0°			6°	0°	6°

Reel Specification-TO-252


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24			0.27	0.009	
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583