

8-bit serial-in,parallel-out shift register

General Description

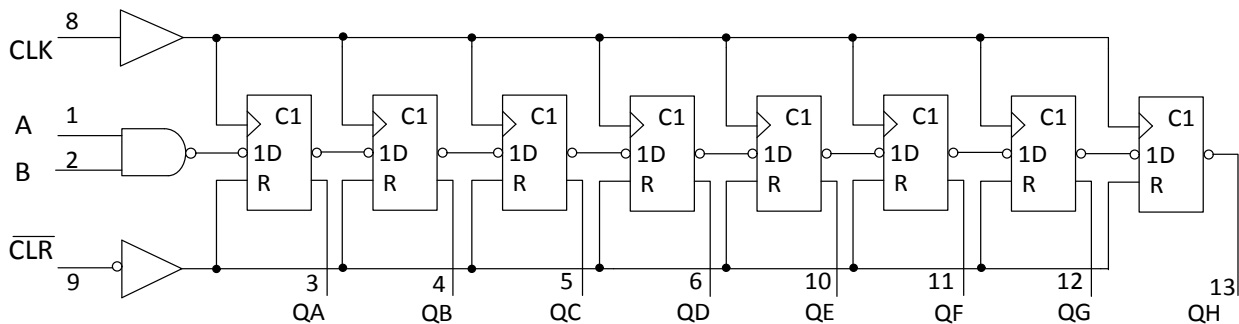
The 74HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (A and B), eight parallel data outputs (QA to QH). Data is entered serially through A or B and either input can be used as an active HIGH enable for data entry through the other input.

Data is shifted on the LOW-to-HIGH transitions of the clock (CLK) input. A LOW on the master reset input (CLR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC.

Features

- 8-bit shift register(serial-in,parallel-out)
- When CLEAR terminal is LOW, QA-QH all are LOW
- Serial data inputs(A、 B) control data.Either input A or B is not able for data entry when in LOW
- QA is LOW in the raise edge of CLOCK terminal
- Package type: DIP14、 SOP14

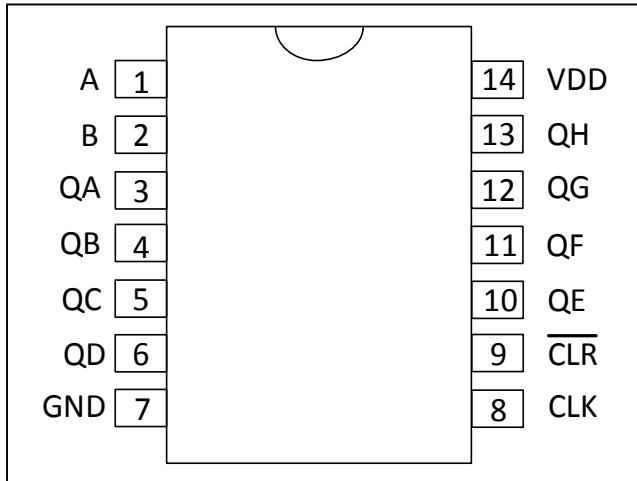
Logic Block Diagram



Note:inputs and outputs correspondng to pin diagram

Figure 1 74HC164 logic block diagram

Pin Configuration



Ordering Information

IC Mode	Package Type	Order NO.
74HC164	DIP-14	164DIP14
74HC164	SOP-14	164SOP14

Pin function Description

DIP-14	Pin Name	Pin Function
1~2	A、B	Serial data input terminals
3~6、10~13	QA、QB、QC、QD、QE、QF、QG、QH	Data output terminals
7	GND	GND
8	CLK	Clock terminal
9	CLR	Clear terminal(active LOW)
14	VDD	Power



Operate Parameters Comparison Table

Name Item	LC	TI	PHI	Note
Drive Current	60mA	50mA	50mA	The driver current of TI is larger than the PHI so that can driver the LED required more current
Operating Frequency	80MHz	36MHz	36MHz	The range of operating frequency is wider than the TI and the PHI
Application	A、B data terminal do not require parallel capacitors to the ground	A、B data terminal require parallel capacitors to the ground		Reduce cost to save a capacitor

Limiting Values

VSS=0V, Ta=25° C unless otherwise specified

Parameter	Symbol	Min	Max	Unit
Logic supply voltage	V _{DD}	-0.5	+6.0	V
Logic input voltage	V _{L1}	-0.5	V _{DD} +0.5	V
Drive output current	I _O	-50		mA
Power dissipation	P _D	400		mW
Operating environment temperature	T _{opt}	-40	+80	°C
Storage temperature	T _{stg}	-65	+150	°C

Normal operating range

VSS=0V, Ta=20° ~27° C unless otherwise specified。

Parameter	Symbol	Min	Type	Max	Unit
Logic supply voltage	V _{DD}	-	5	-	V
High-level input voltage	V _{IH}	0.7V _{DD}	-	V _{DD}	V
Low-level input voltage	V _{IL}	0	-	0.3V _{DD}	V
Input transfer time	T _t	400	500	1000	ns



LC74HC164 Compare With SN74HC164

VSS=6V, Ta=25° C unless otherwise specified

Character	Symbol	Condition	Code Value		LC74C164	SN74HC164	Unit
			Min	Max	25°C		
Supply current	V _{DD}	V _I =0V、6V , output no load	-	80	2	2	uA
Hign-level input voltage	V _{IH}		4.2	-	4.2	4.2	V
Low-level input voltage	V _{IL}		-	1.35	1.35	1.35	V
Hign-level output voltage	V _{OH}	I _{OH} =-5.2mA	5.34	-	5.99	5.99	V
Low-level output voltage	V _{OL}	I _{OL} =5.2mA		0.33	0.05	0.05	V
Input sink current	I _I	V _{IL} =0V ,V _{IH} =6V	-0.1	0.1	0.01	0.01	uA
Clock rising edge to data valid time	T _A		-	30	2	-	ns
Data to clock setup time	T _{SD}		17	-	5	5	ns
Operating frequency	f _{MAX}		-	100	80	36	MHz
Drive cureent	I _O	V _{DD} =5V,V _{OH} =3.0V	58	65	60	50	mA



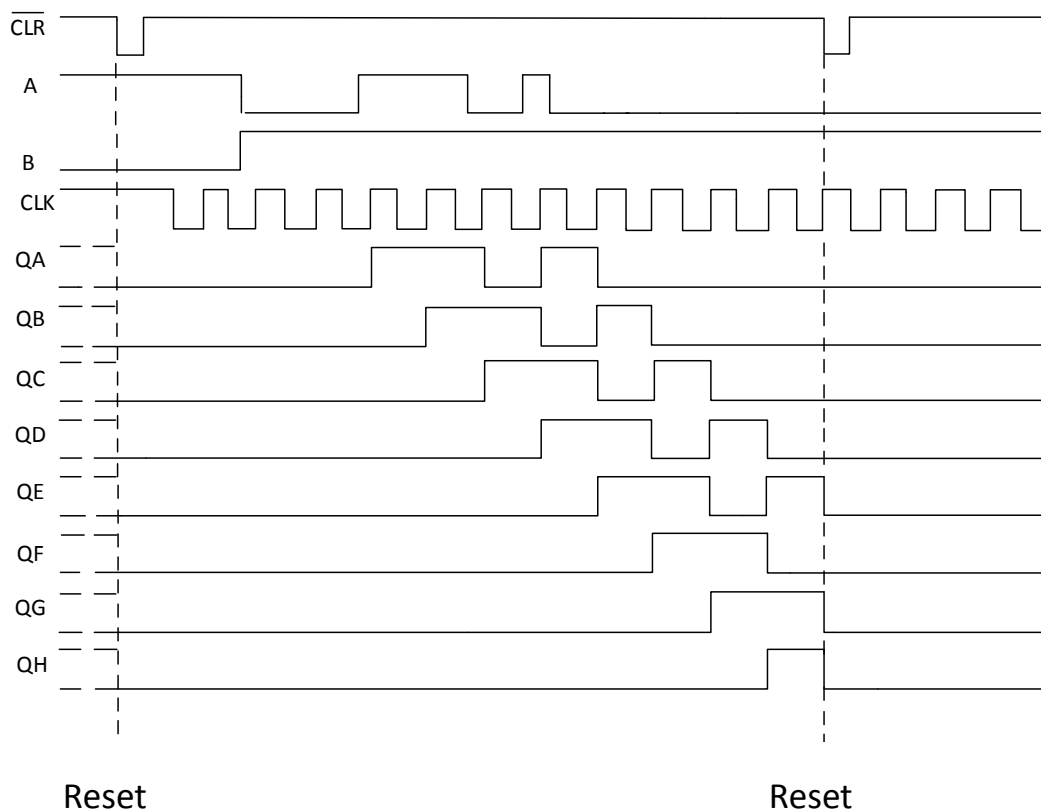
Function Table

Input				Output		
$\overline{\text{CLR}}$	CLK	A	B	QA	QB-----QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	1	H	H	H	QAn	QGn
H	1	L	X	L	QAn	QGn
H	1	X	L	L	QAn	QGn

QA0---QH0 show the states when the raise edge of CLK have not arrived to QA-QH.QAn---QGn show the states have got to the edge of CLK.

QA---QG states before the raise edge of CLK show it have one shift for one CLK arrived.

Sequence Chart



Referenced Measure Data

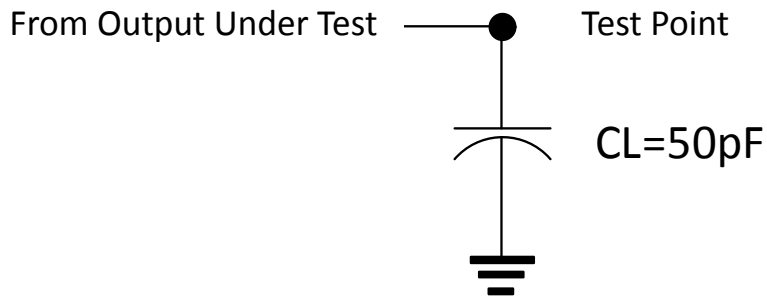


Figure 1 Load Current

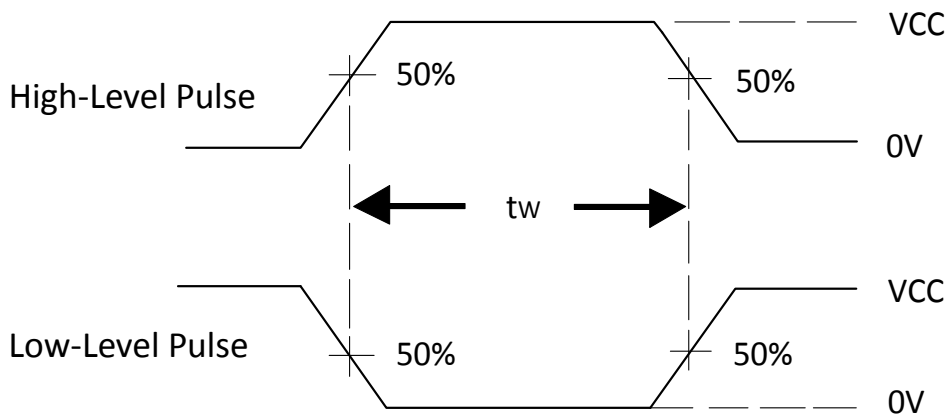


Figure 2 Voltage Waveforms Pulse Durations

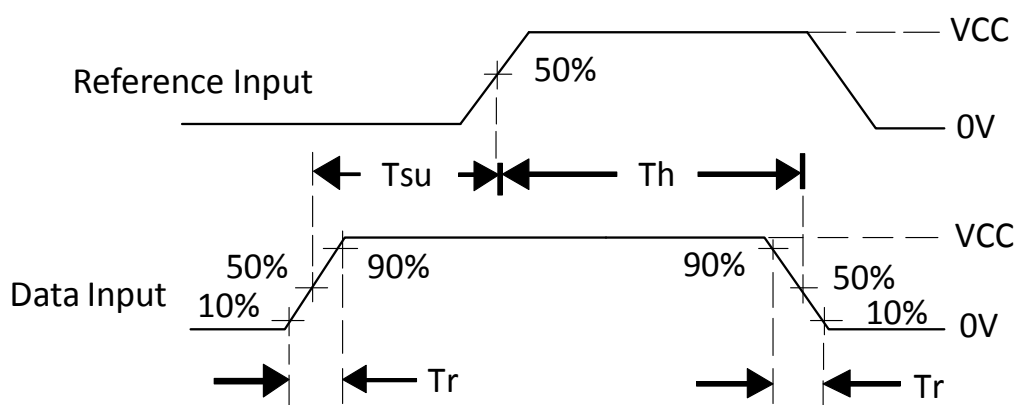


Figure 3 Voltage Waveforms Setup And Input Rise And Fall Times

Referenced Measure Data (Continued)

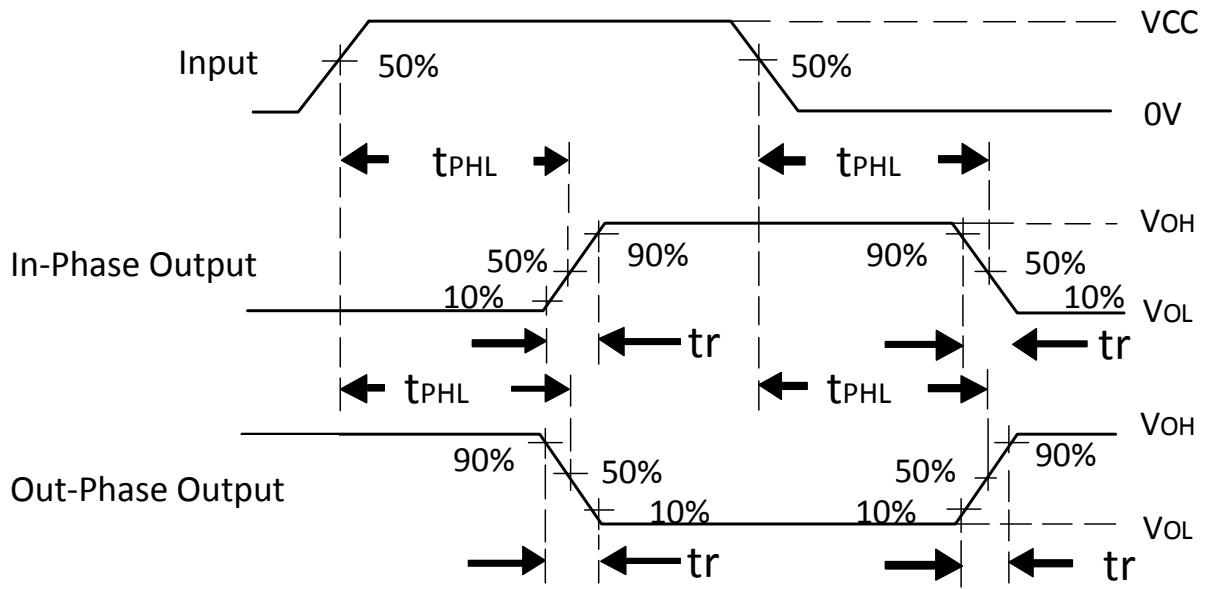
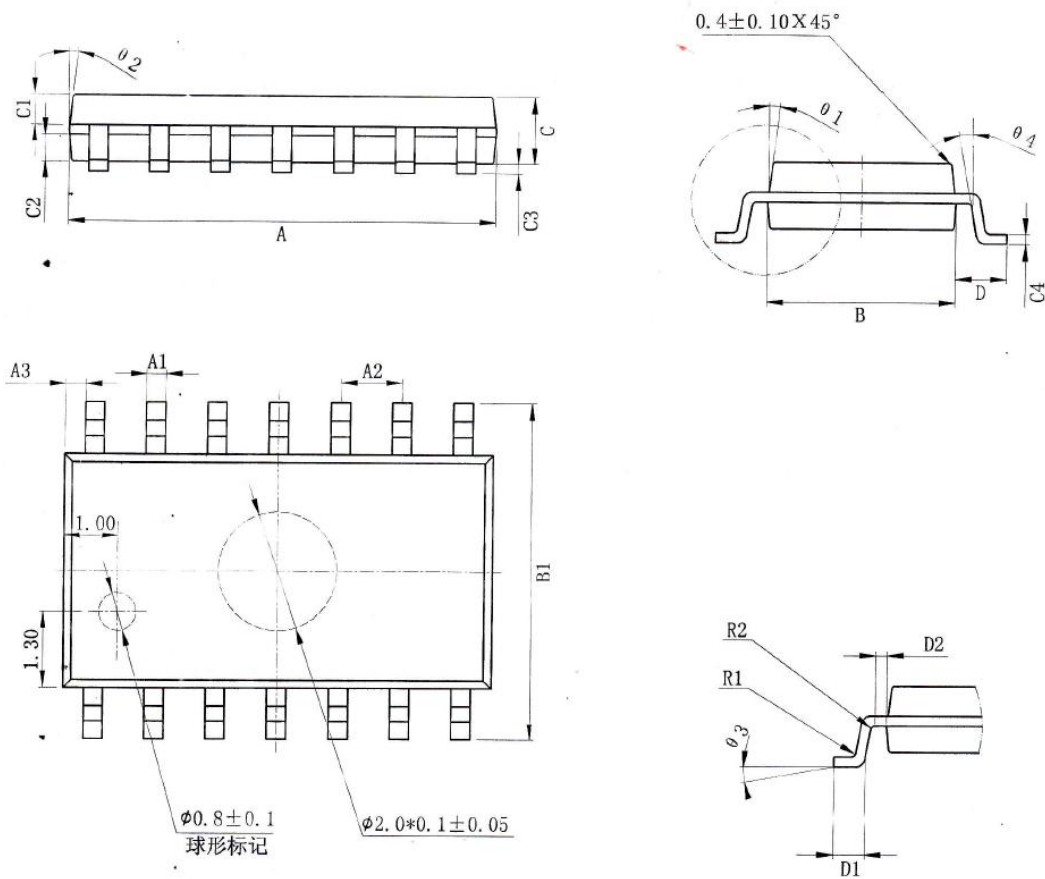


Figure 4 Voltage Waveforms Propagation Delay And Output Transition Times



Package Outline

1、SOP14 Package

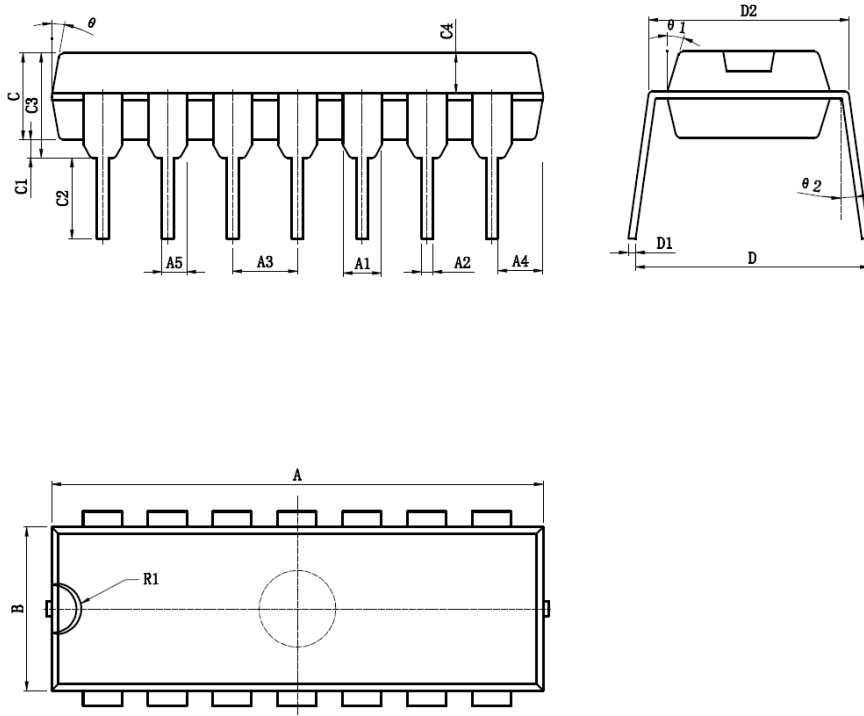


Symbol	Size (mm)		Symbol	Size (mm)	
	Min	Max		Min	Max
A	8.55	8.75	C4	0.203	0.233
A1	0.356	0.456	D	0.95	1.15
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.20TYP	
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
C	1.40	1.60	$\theta 1$	8°~12°TYP	
C1	0.60	0.70	$\theta 2$	8°~12°TYP	
C2	0.52	0.62	$\theta 3$	0°~8°	
C3	0.05	0.25	$\theta 4$	4°~12°	



Package Outline (Continued)

2、DIP14 Package



Symbol	Size (mm)		Symbol	Size (mm)	
	Min	Max		Min	Max
A	19.00	19.20	C3	3.85	4.45
A1	1.524TYP		C4	1.40	4.50
A2	0.41	0.51	D	8.20	8.80
A3	2.54TYP		D1	0.20	0.35
A4	1.70TYP		D2	7.74	8.00
A5	0.99TYP		θ	10°TYP	
B	6.30	6.50	$\theta 1$	17°TYP	
C	3.00	3.20	$\theta 2$	6°TYP	
C1	0.51TYP		R1	1.27TYP	
C2	3.00	3.60			