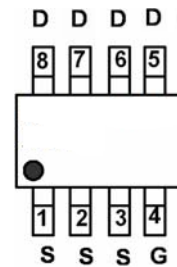




PIN CONFIGURATION

(SOP-8)



Description

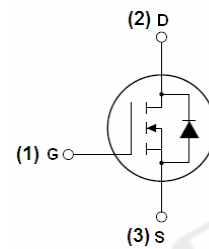
The FIR14N10DG uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of R\_DS(ON) and Q\_g. This device is ideal for high-frequency switching and synchronous rectification.

General Features

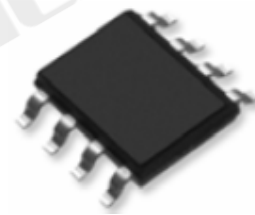
- V\_DS =100V, I\_D =14A
R\_DS(ON)=8.8mΩ (typical) @ V\_GS=10V
R\_DS(ON)=9.8mΩ (typical) @ V\_GS=4.5V
• Excellent gate charge x R\_DS(on) product(FOM)
• Very low on-resistance R\_DS(on)
• 150 °C operating temperature
• Pb-free lead plating
• 100% UIS tested

Application

- DC/DC Converter
• Ideal for high-frequency switching and synchronous rectification



N-Channel MOSFET



SOP-8 top view

Absolute Maximum Ratings (T\_A=25°C unless otherwise noted)

Table with 4 columns: Parameter, Symbol, Limit, Unit. Rows include Drain-Source Voltage, Gate-Source Voltage, Drain Current-Continuous, Pulsed Drain Current, Maximum Power Dissipation, etc.

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	36	$^{\circ}C/W$
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**Electrical Characteristics ( $T_A=25^{\circ}C$  unless otherwise noted)**

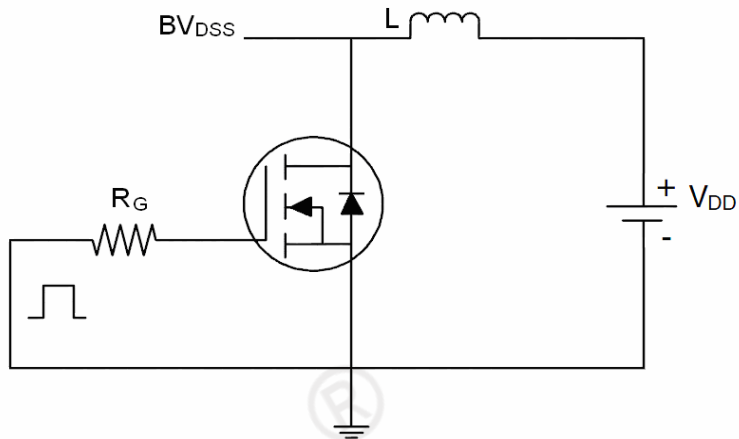
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=14A$	-	8.8	11	m $\Omega$
		$V_{GS}=4.5V, I_D=14A$	-	9.8	13	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=14A$	45	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	4200	5480	PF
Output Capacitance	$C_{oss}$		-	354	425	PF
Reverse Transfer Capacitance	$C_{rss}$		-	23	30	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=14A$ $V_{GS}=10V, R_G=1.6\Omega$	-	14	-	nS
Turn-on Rise Time	$t_r$		-	9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	nS
Turn-Off Fall Time	$t_f$		-	5	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=14A,$ $V_{GS}=10V$	-	58	-	nC
Gate-Source Charge	$Q_{gs}$		-	15	-	nC
Gate-Drain Charge	$Q_{gd}$		-	7.8	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=14A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	14	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	101	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	193	-	nC

**Notes:**

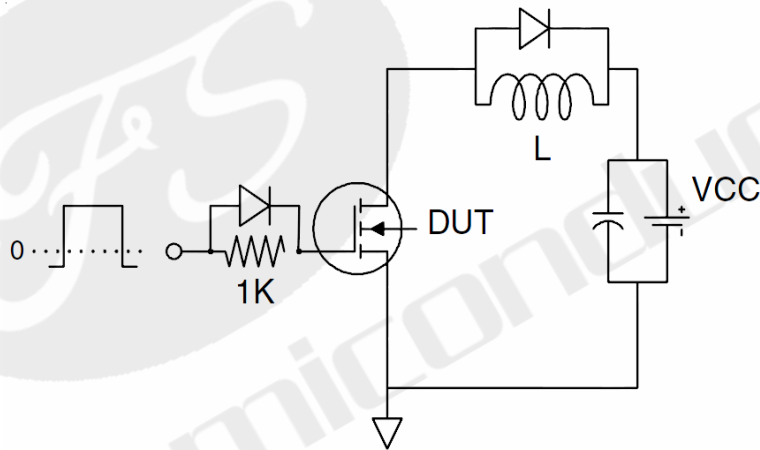
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

**Test Circuit**

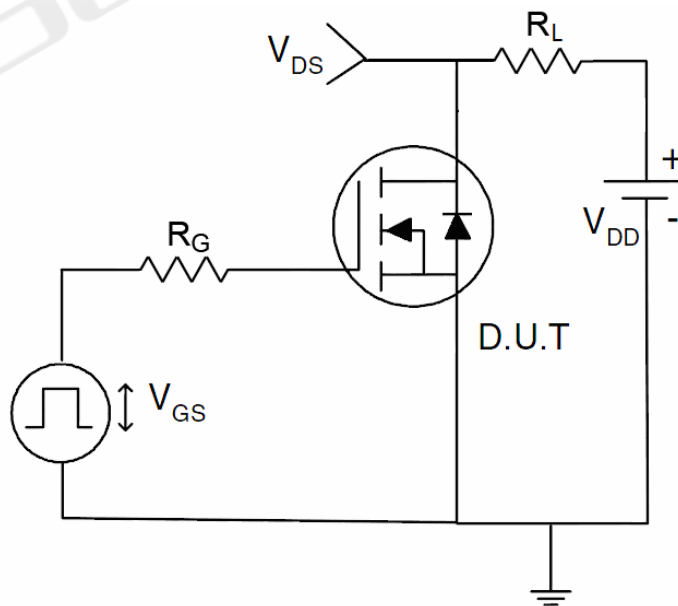
**1) E<sub>AS</sub> test Circuit**



**2) Gate charge test Circuit**



**3) Switch Time Test Circuit**





### Typical Electrical and Thermal Characteristics

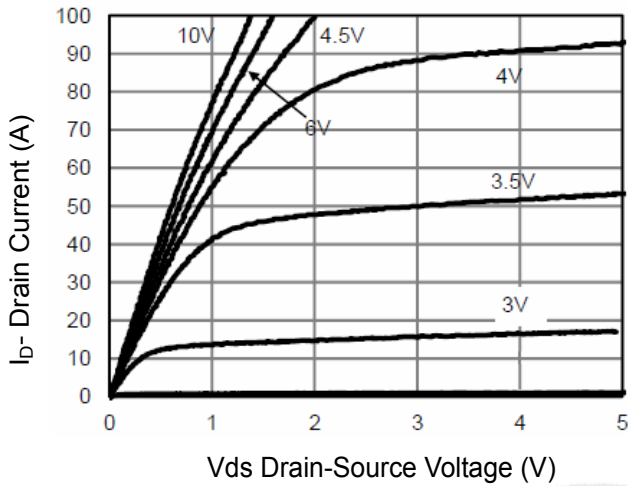


Figure 1 Output Characteristics

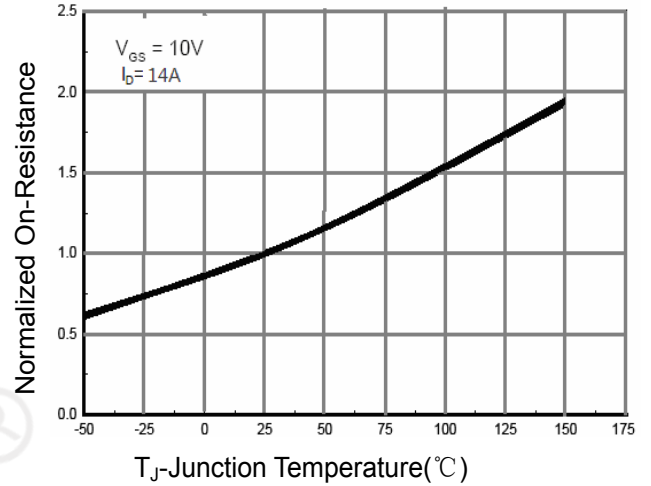


Figure 4 Rds(on)-Junction Temperature

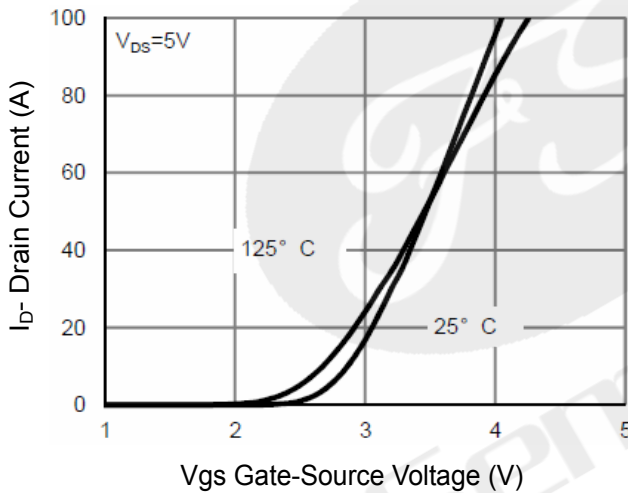


Figure 2 Transfer Characteristics

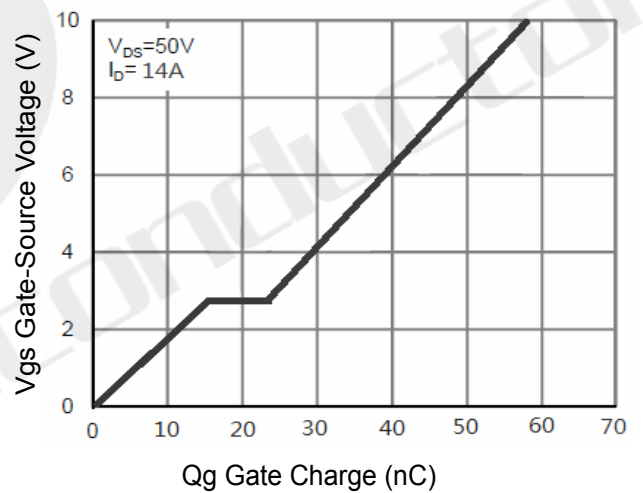


Figure 5 Gate Charge

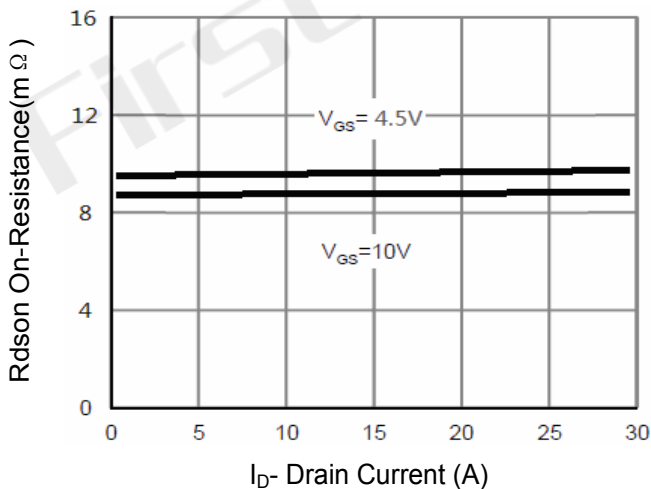


Figure 3 Rds(on)- Drain Current

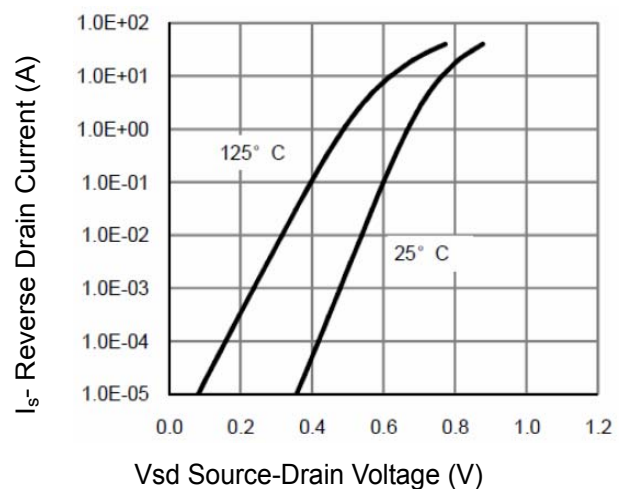


Figure 6 Source- Drain Diode Forward

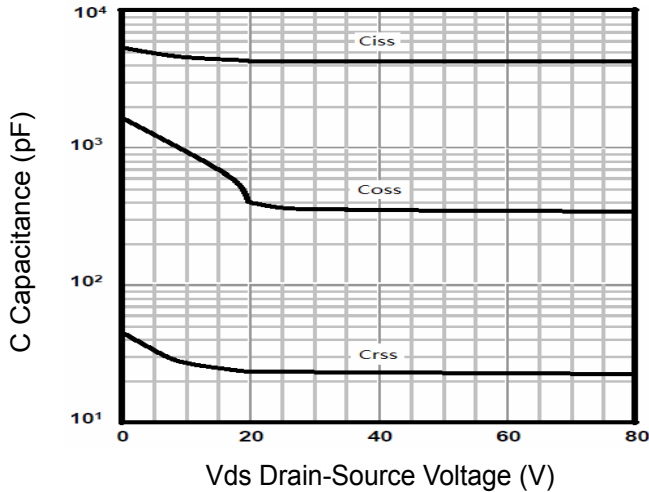


Figure 7 Capacitance vs Vds

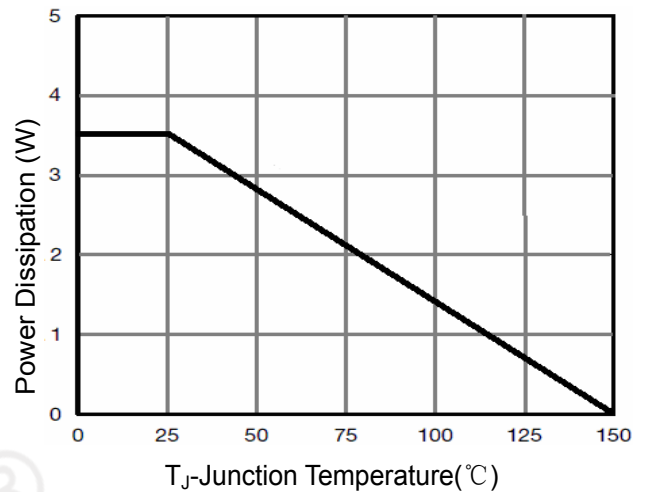


Figure 9 Power De-rating

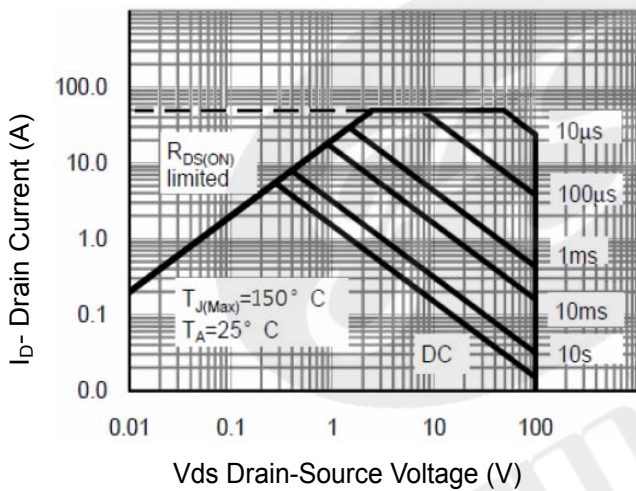


Figure 8 Safe Operation Area

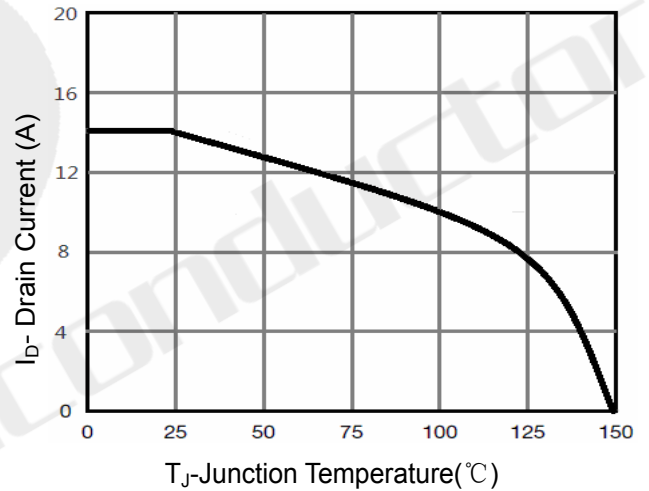


Figure 10 Current De-rating

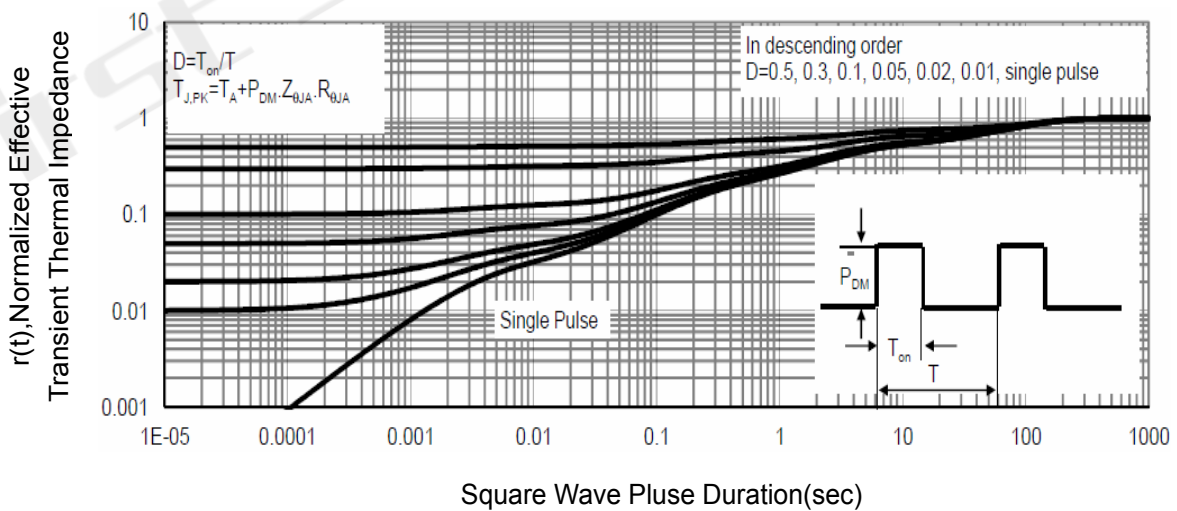
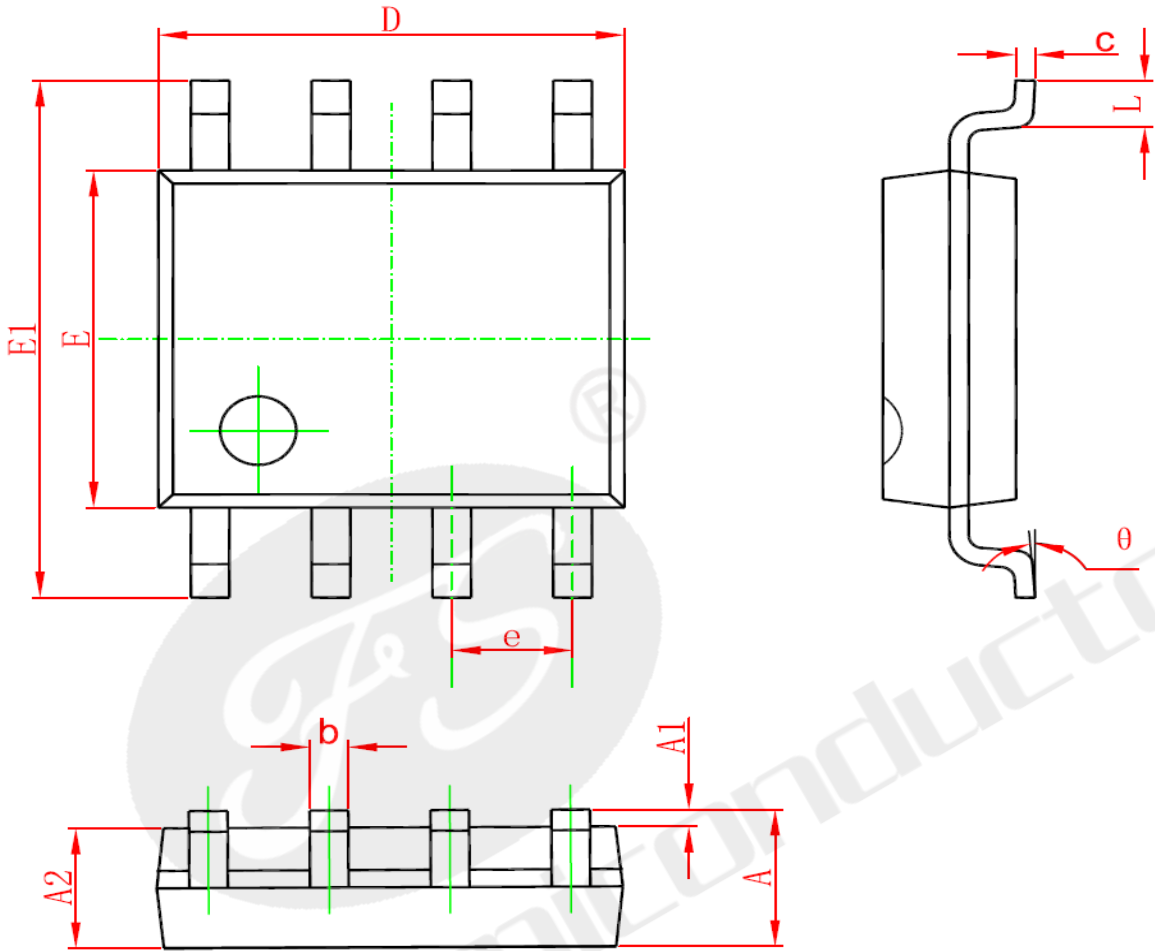


Figure 11 Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

**ATTACHMENT**

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	