FIR15P055BPG

P-Channel Enhancement Mode Power Mosfet

Descripton

The FIR15P055BPG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.
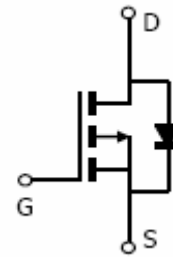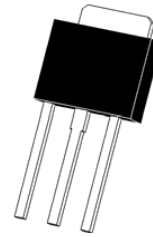
General Features

● V_{DS} =-55V,I_D =-15A

$R_{DS(ON)}$ < 75mΩ @ V_{GS}=-10V

● High density cell design for ultra low Rdson

● Fully characterized avalanche voltage and current

● Excellent package for good heat dissipation

Application

● Power switching application

● Hard switched and high frequency circuits

● DC-DC Conveter

PIN Connection   TO-251

Schematic diagram

Y	= Year
A	= Assembly Location
WW	= Work Week
FIR15P055BP	= Specific Device Code

Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR15P055BP	FIR15P055BPG	TO-251	-	-	-

Absolute Maximum Ratings (T$_C$=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-55	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-15	A
Drain Current-Continuous(T$_C$=100℃)	I_D (100℃)	-10	A
Pulsed Drain Current	I_{DM}	-50	A
Maximum Power Dissipation	P_D	50	W
Derating factor		0.73	W/℃
Single pulse avalanche energy [Note 5]	E_{AS}	110	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case[Note 2]	$R_{θJC}$	2.5	℃/W

FIR15P055BPG

Electrical Characteristics (T_C=25℃ unless otherwise noted)

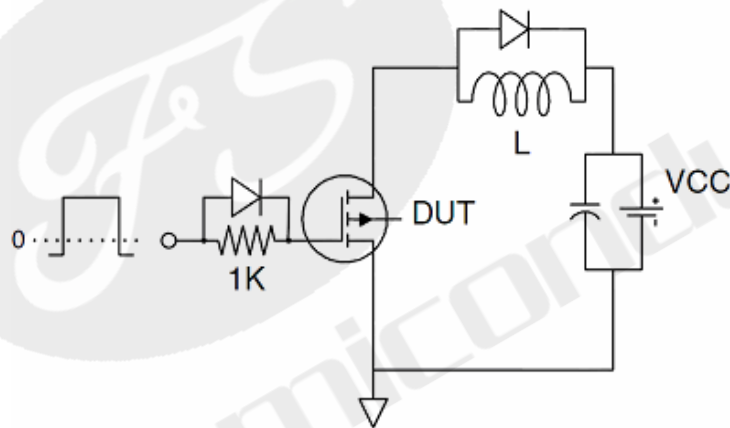| Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV$_{DSS}$	V$_{GS}$=0V I$_D$=-250μA	-55	-	-	V
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$=-55V,V$_{GS}$=0V	-	-	1	μA
Gate-Body Leakage Current	I$_{GSS}$	V$_{GS}$=±20V,V$_{DS}$=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$=V$_{GS}$,I$_D$=-250μA	-1.5	-2.6	-3.5	V
Drain-Source On-State Resistance	R$_{DS(ON)}$	V$_{GS}$=-10V, I$_D$=5A	-	60	75	mΩ
Forward Transconductance	g$_{FS}$	V$_{DS}$=-15V,I$_D$=-5A	16	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C$_{Iss}$	V$_{DS}$=-20V,V$_{GS}$=0V, F=1.0MHz	-	1450	-	PF
Output Capacitance	C$_{oss}$		-	145	-	PF
Reverse Transfer Capacitance	C$_{rss}$		-	110	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t$_{d(on)}$	V$_{DD}$=-30V, R$_L$=30Ω V$_{GS}$=-10V,R$_{GEN}$=6Ω	-	8	-	nS
Turn-on Rise Time	t$_r$		-	9	-	nS
Turn-Off Delay Time	t$_{d(off)}$		-	65	-	nS
Turn-Off Fall Time	t$_f$		-	30	-	nS
Total Gate Charge	Q$_g$	V$_{DS}$=-30V,I$_D$=-5A, V$_{GS}$=10V	-	26	-	nC
Gate-Source Charge	Q$_{gs}$		-	4.5	-	nC
Gate-Drain Charge	Q$_{gd}$		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V$_{SD}$	V$_{GS}$=0V,I$_S$=-5A	-	-	-1.2	V
Diode Forward Current (Note 2)	I$_S$		-	-	-15	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

5. EAS condition：Tj=25℃,V$_{DD}$=-30V,V$_G$=-10V,L=0.5mH,Rg=25Ω
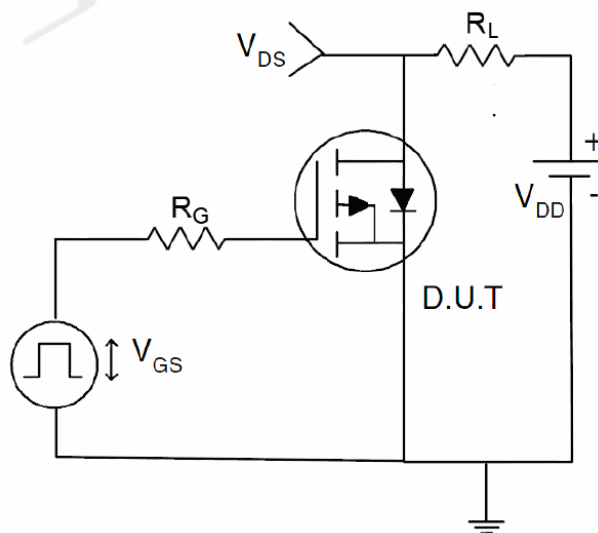
Test circuit

1) E$_{AS}$ test Circuits

2) Gate charge test Circuit:

3) Switch Time Test Circuit：

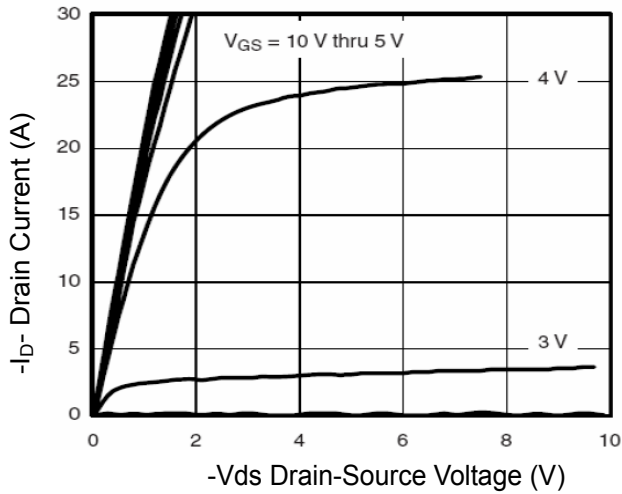## Typical Electrical and Thermal Characteristics (Curves)
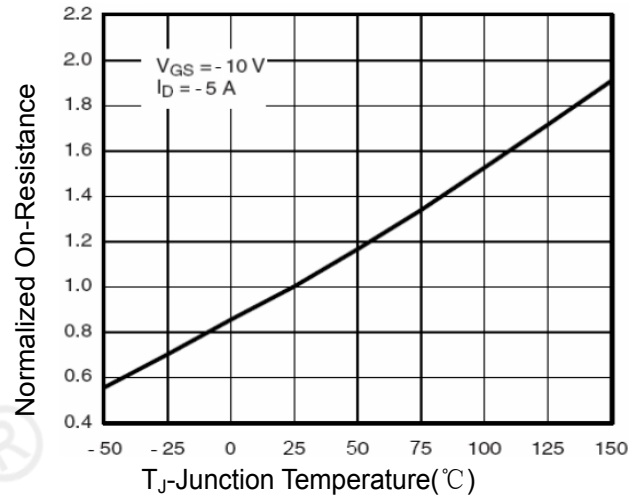

Figure 1 Output Characteristics
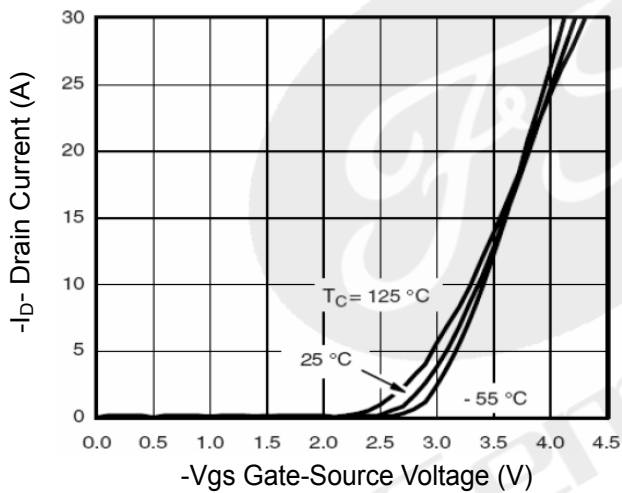

Figure 4 Rdson-JunctionTemperature

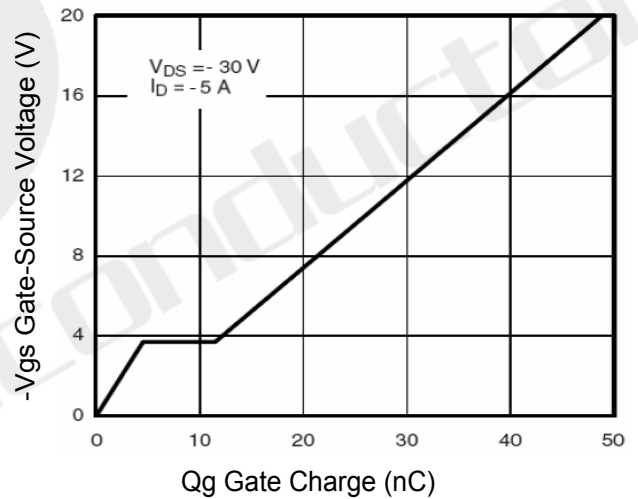

Figure 2 Transfer Characteristics
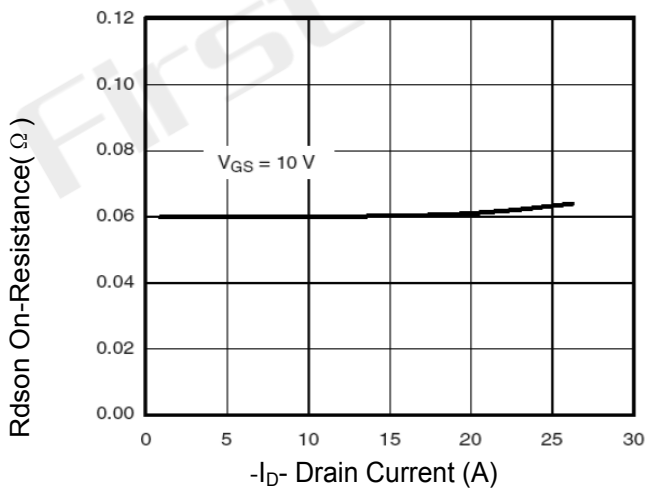

Figure 5 Gate Charge
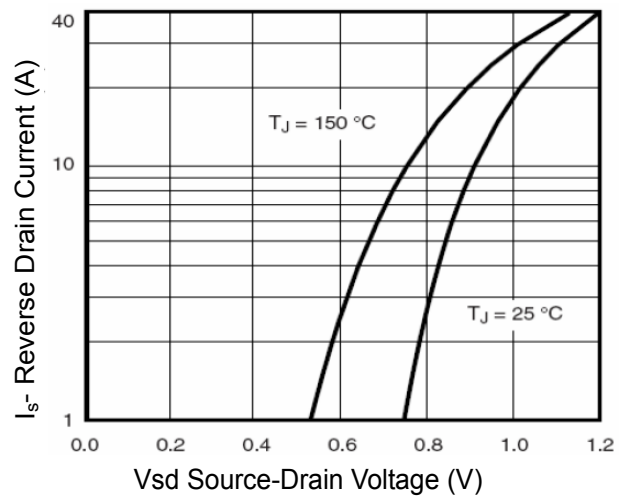

Figure 3 Rdson- Drain Current

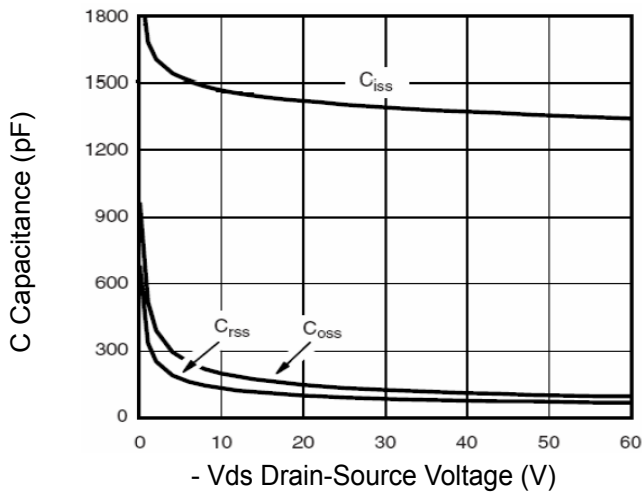**Figure 6 Source- Drain Diode Forward**
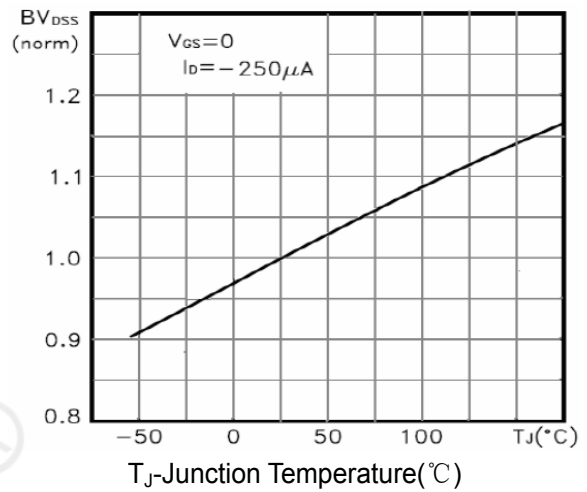
Figure 7 Capacitance vs Vds
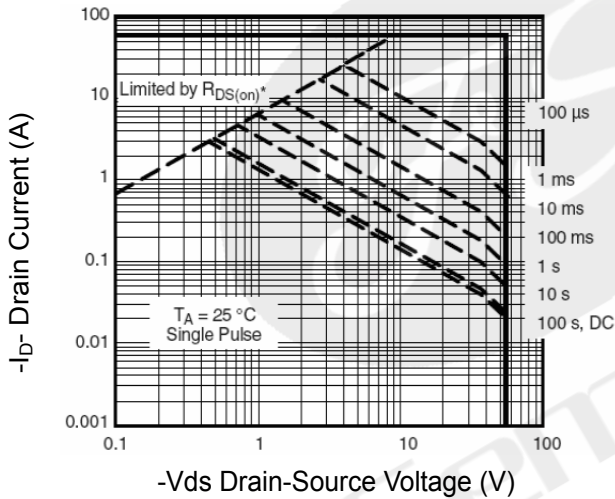

Figure 9 BV$_{DSS}$ vs Junction Temperature

Figure 8 Safe Operation Area
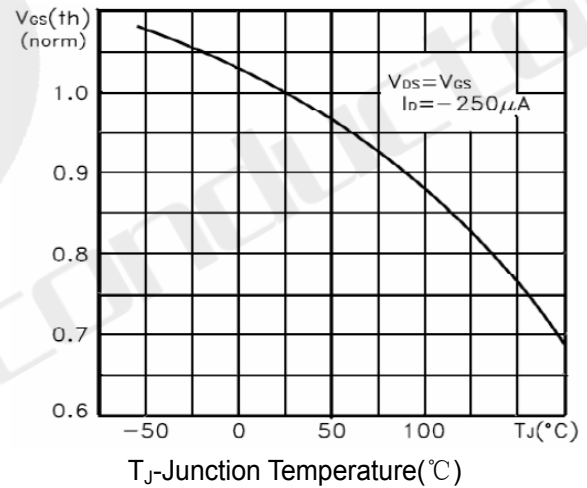

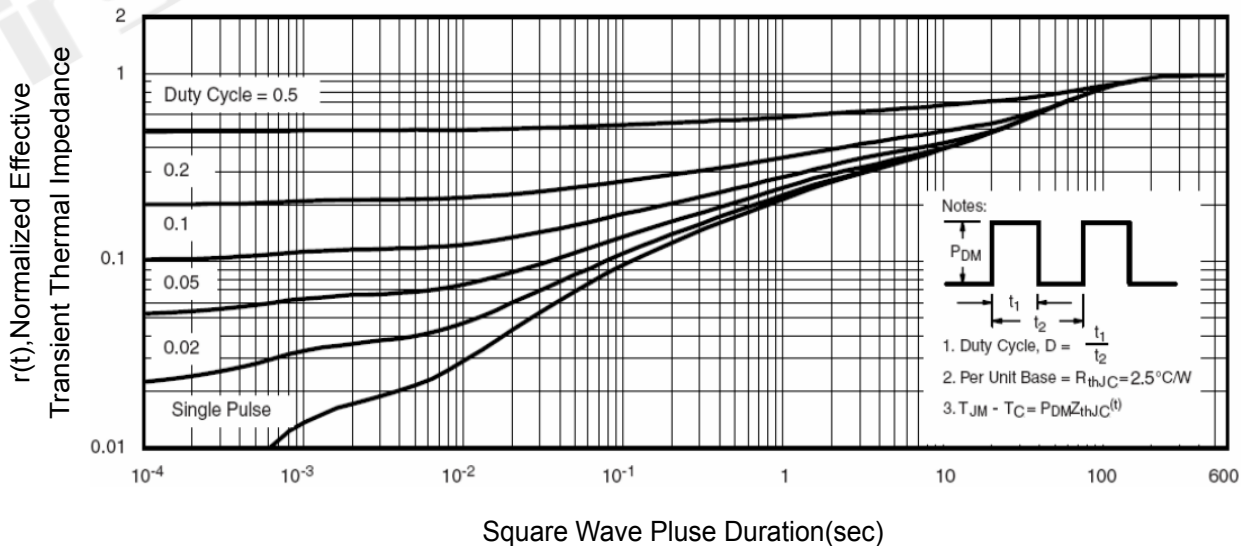
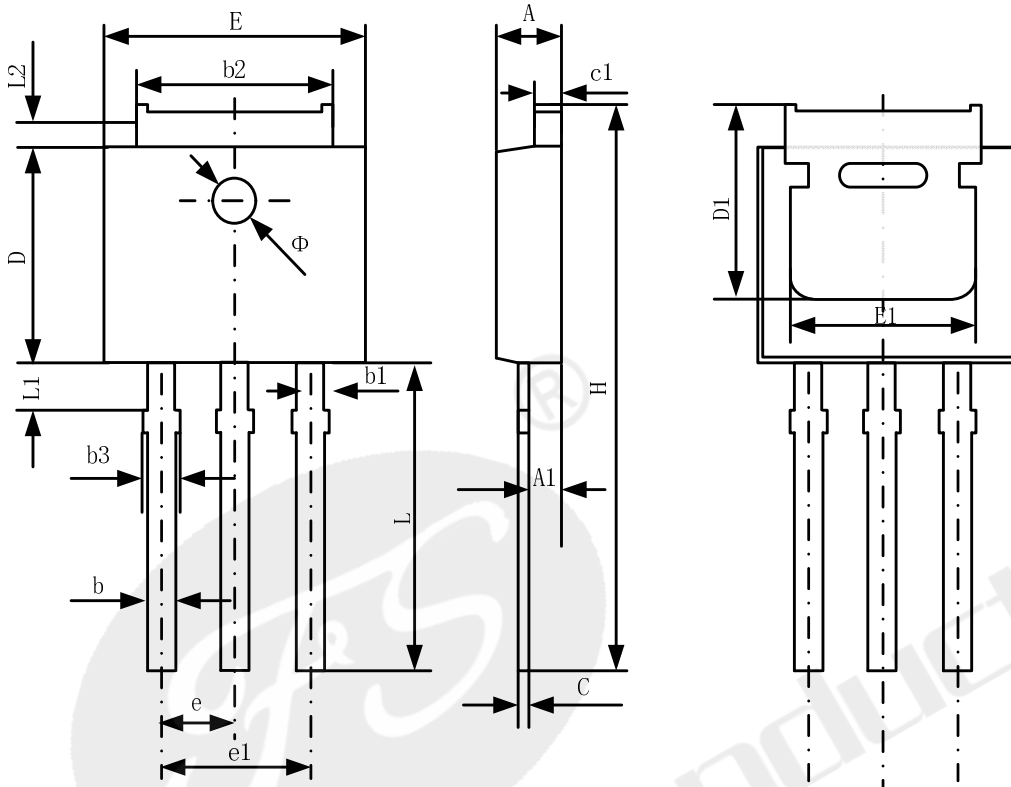**Figure 10 V$_{GS(th)}$ vs Junction Temperature**

Figure 11 Normalized Maximum Transient Thermal Impedance

Package Information

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.35	0.087	0.093
A1	0.90	1.10	0.035	0.043
b	0.56	0.69	0.022	0.027
b1	0.77	0.90	0.030	0.035
b2	5.23	5.43	0.206	0.214
b3		1.05		0.041
C	0.46	0.59	0.018	0.023
c1	0.46	0.59	0.018	0.023
D	6.00	6.20	0.236	0.244
D1	5.20	--	0.205	--
E	6.50	6.70	0.256	0.264
E1	4.60	5.00	0.181	0.197
e	2.24	2.34	0.088	0.092
e1	4.47	4.67	0.176	0.184
H	16.18	16.78	0.637	0.661
L	9.00	9.60	0.354	0.378
L1	0.95	1.35	0.037	0.053
L2	0.90	1.25	0.035	0.049

First Semiconductor

Declaration

● FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice!
  Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.

● Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety
  standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!

● Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	