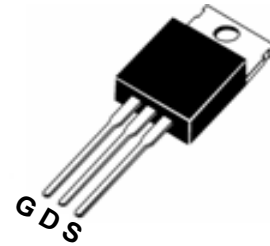




PIN Connection TO-220AB



Description

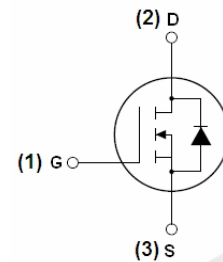
The FIR20N15PG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 150V, I_D = 20A$
 $R_{DS(ON)} < 85m\Omega @ V_{GS} = 10V$ (Typ: 70m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Boost converters
- LED backlighting
- Uninterruptible power supply



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR20N15P = Specific Device Code

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR20N15P	FIR20N15PG	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	20	A
$I_D(100^\circ C)$	Drain Current-Continuous($TC = 100^\circ C$)	14	A
I_{DM}	Pulsed Drain Current	40	A
P_D	Maximum Power Dissipation	75	W
	Derating factor	0.5	W/ $^\circ C$
E_{AS}	Single pulse avalanche energy ^(Note 5)	200	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$



Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	2.0	$^{\circ}\text{C}/\text{W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

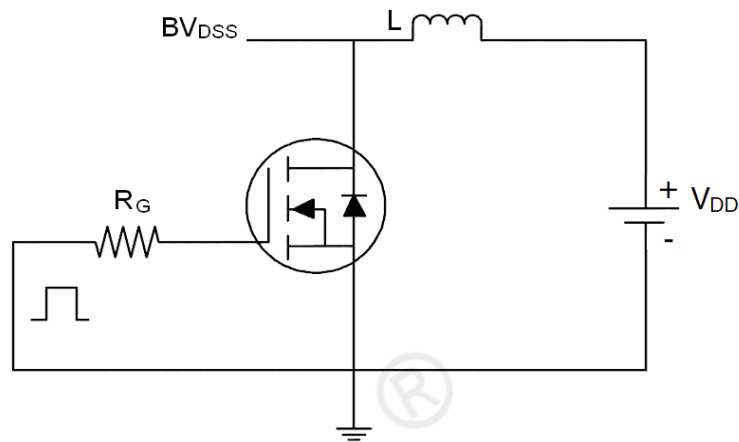
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	150	165	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=150V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3.4	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=10A$	-	70	85	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	-	20	-	S
Dynamic Characteristics ^(Note 4)						
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2000	-	PF
C_{oss}	Output Capacitance		-	290	-	PF
C_{rss}	Reverse Transfer Capacitance		-	180	-	PF
Switching Characteristics ^(Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=75V, R_L=5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	10.5	-	nS
t_r	Turn-on Rise Time		-	5.5	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	14.5	-	nS
t_f	Turn-Off Fall Time		-	3	-	nS
Q_g	Total Gate Charge	$V_{DS}=75V, I_D=10A,$ $V_{GS}=10V$	-	17	-	nC
Q_{gs}	Gate-Source Charge		-	4	-	nC
Q_{gd}	Gate-Drain Charge		-	4.4	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage ^(Note 3)	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
I_S	Diode Forward Current ^(Note 2)	-	-	-	20	A
t_{rr}	Reverse Recovery Time	$T_J = 25^{\circ}\text{C}, I_F = 10A$	-	32	-	nS
Q_{rr}	Reverse Recovery Charge	$di/dt = 100A/\mu s$ ^(Note 3)	-	53	-	nC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

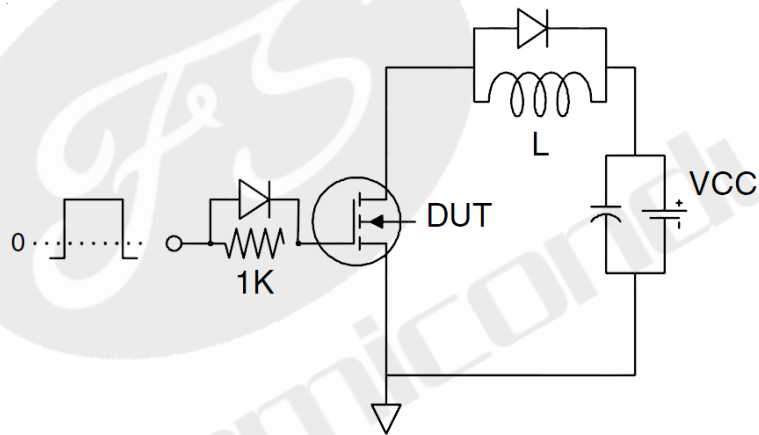
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

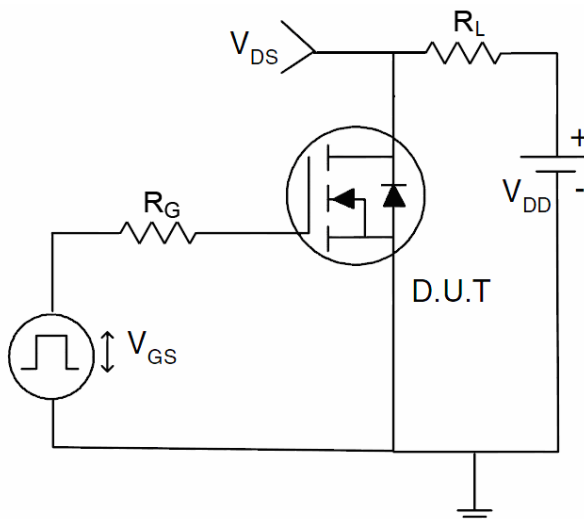
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

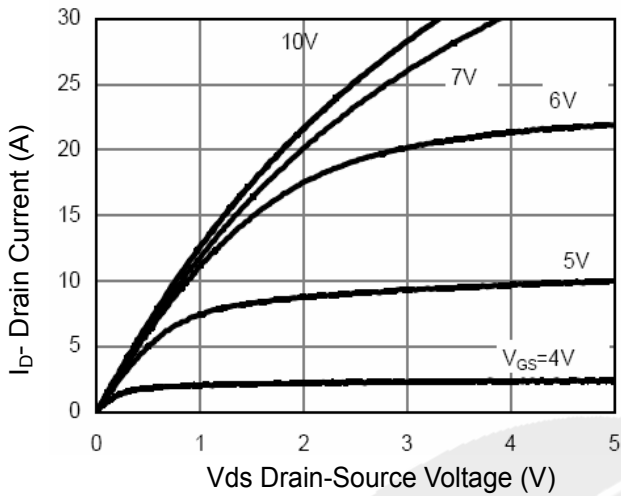


Figure 1 Output Characteristics

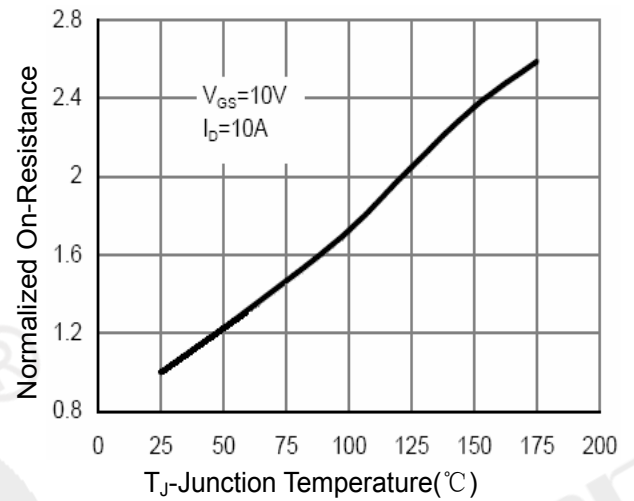


Figure 4 R_{dson} -Junction Temperature

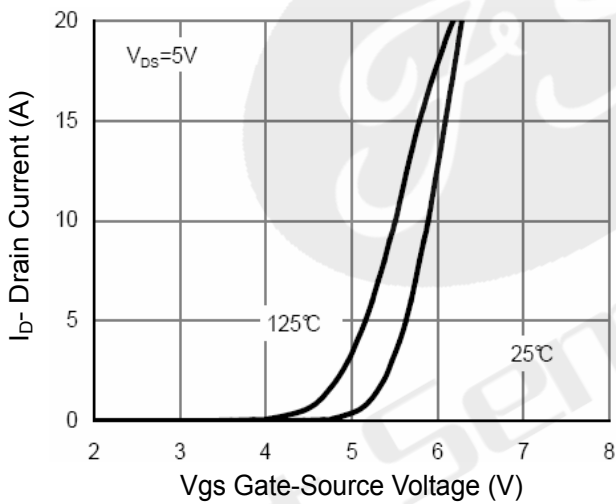


Figure 2 Transfer Characteristics

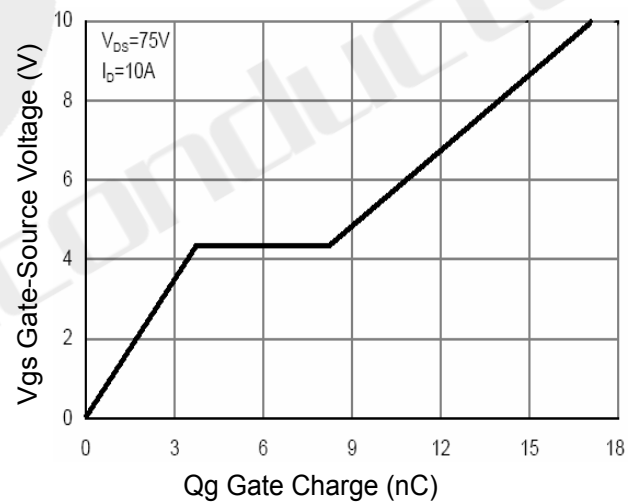


Figure 5 Gate Charge

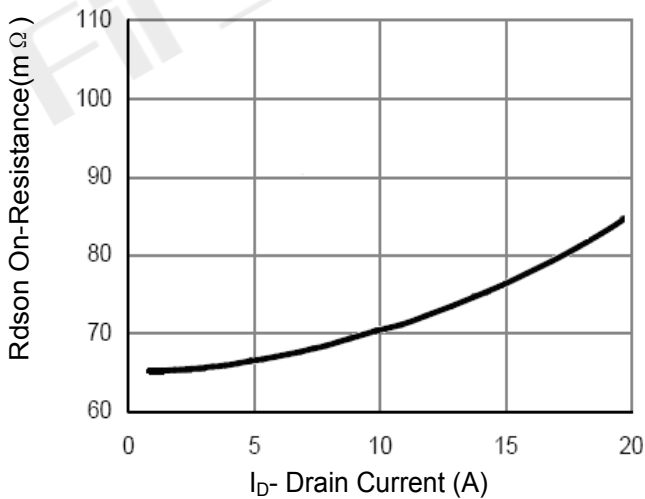


Figure 3 R_{dson} - Drain Current

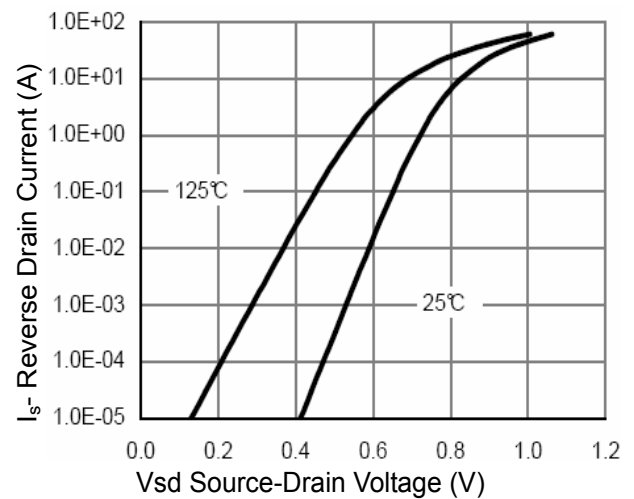


Figure 6 Source- Drain Diode Forward

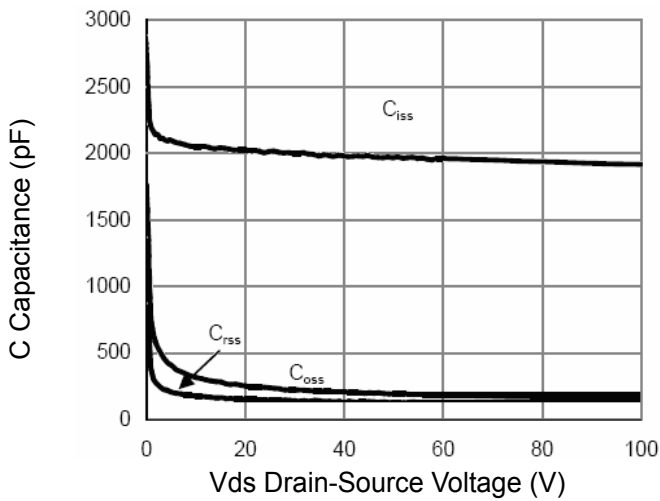


Figure 7 Capacitance vs Vds

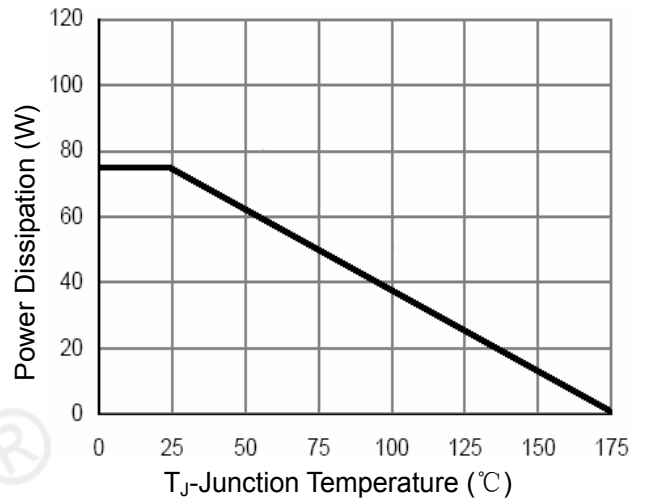


Figure 9 Power De-rating

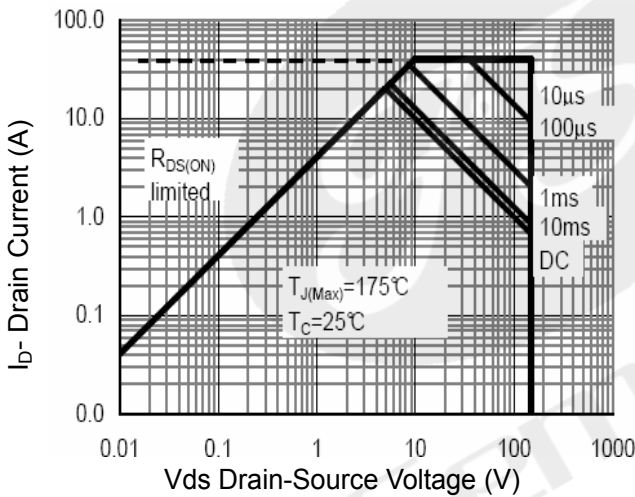


Figure 8 Safe Operation Area

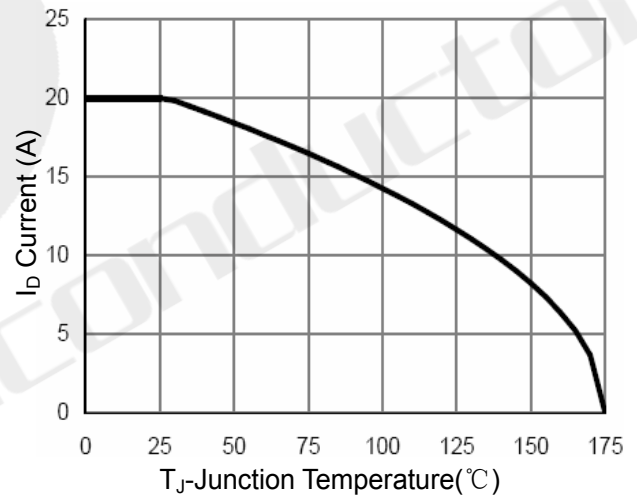


Figure 10 Id Current- Junction Temperature

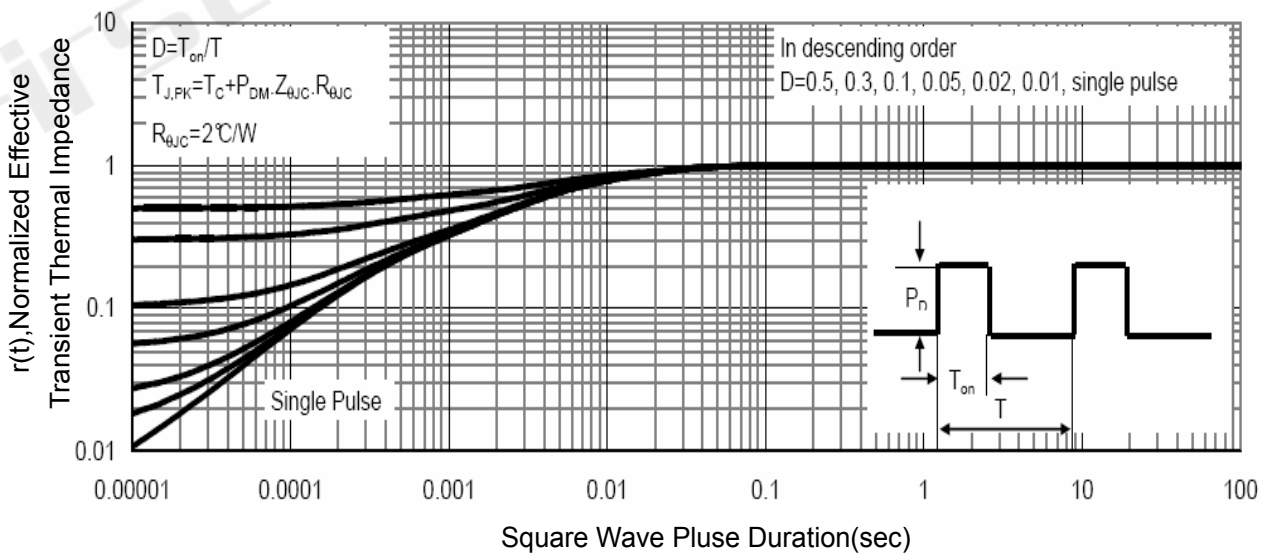
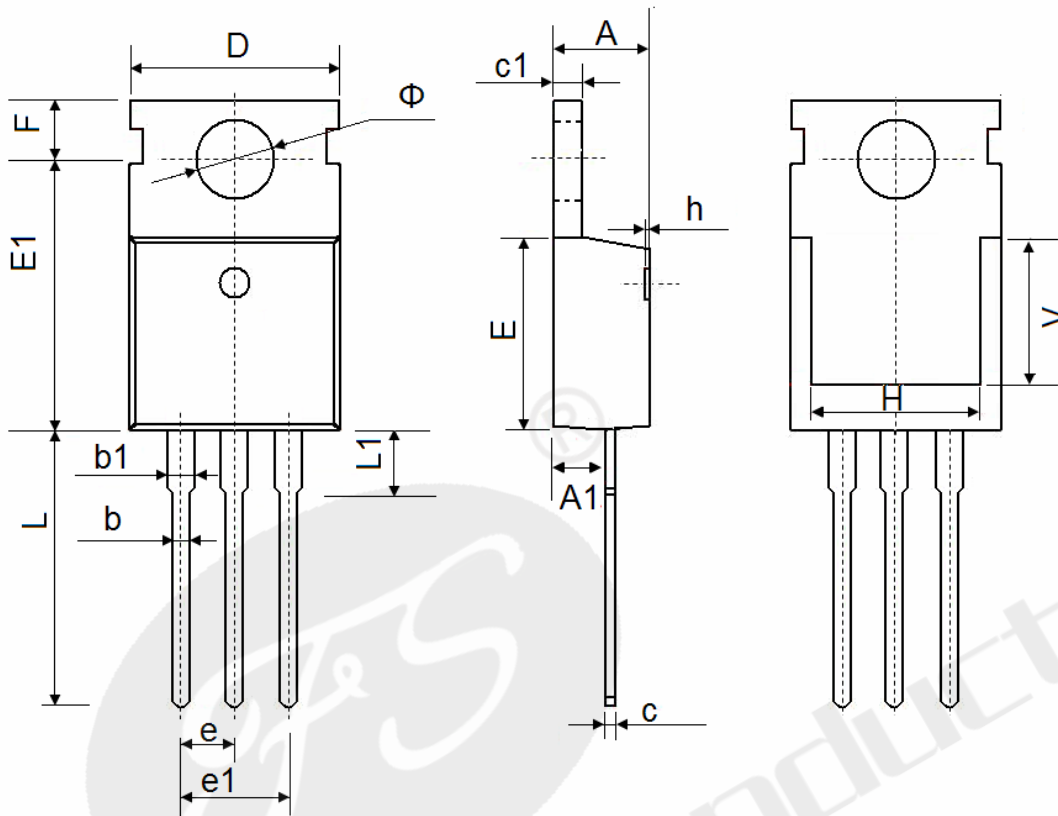


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220AB Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	