

Description

The FIR57N10ANG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

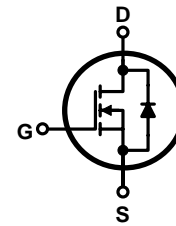
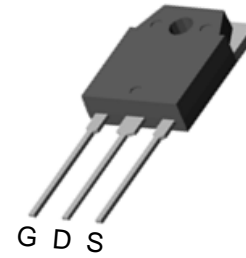
General Features

- $V_{DS} = 100V, I_D = 57A$
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=10V$ (Typ:11.7m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

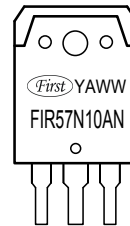
Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

PIN Connection TO-3P



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR57N10AN = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR57N10AN	FIR57N10ANG	TO-3P	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	57	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	40	A
Pulsed Drain Current	I_{DM}	190	A
Maximum Power Dissipation	P_D	180	W
Derating factor		1.2	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	580	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	0.83	$^{\circ}C/W$
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Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

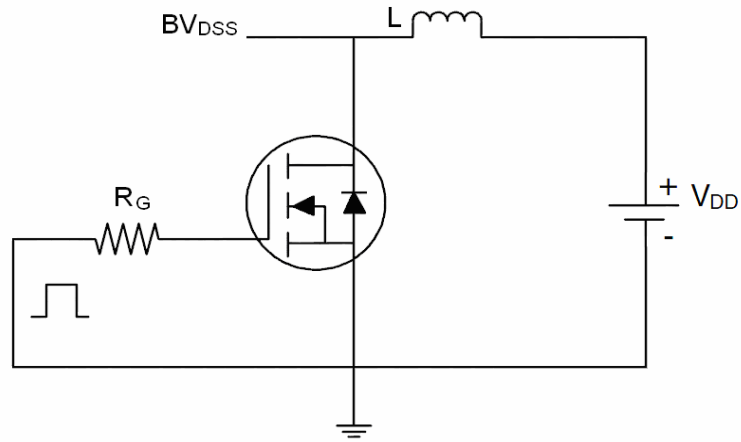
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=28A$	-	11.7	16	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=28A$	32	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	2700	-	PF
Output Capacitance	C_{oss}		-	350	-	PF
Reverse Transfer Capacitance	C_{rss}		-	150	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=28A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	12	-	nS
Turn-on Rise Time	t_r		-	55	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	47	-	nS
Total Gate Charge	Q_g	$V_{DS}=80V, I_D=28A,$ $V_{GS}=10V$	-	95	-	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain Charge	Q_{gd}		-	25	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=28A$	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	57	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 28A$	-	140	220	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note3)	-	650	1000	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

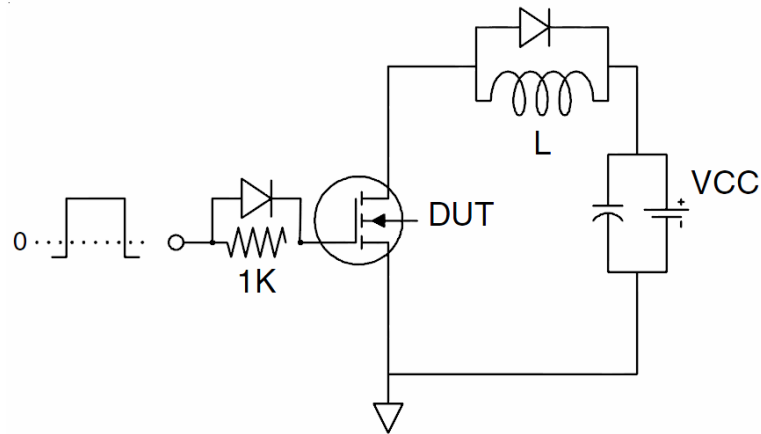
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

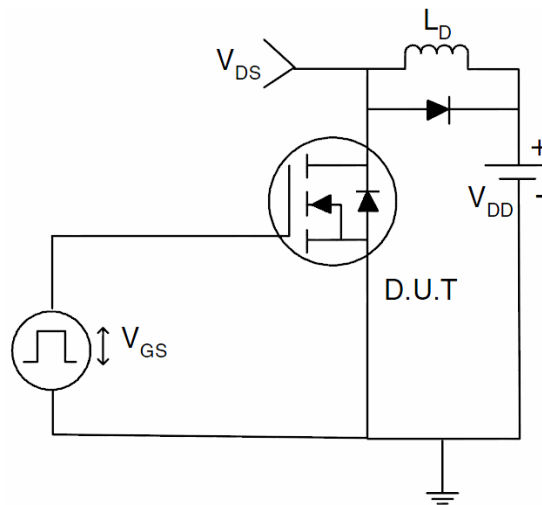
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical And Thermal Characteristics(Curves)

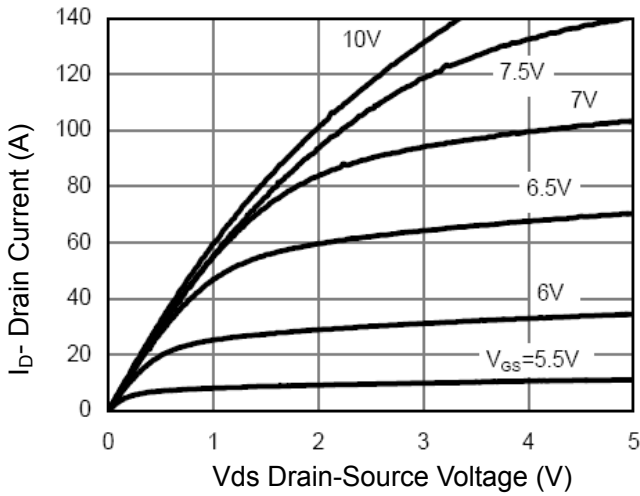


Figure 1 Output Characteristics

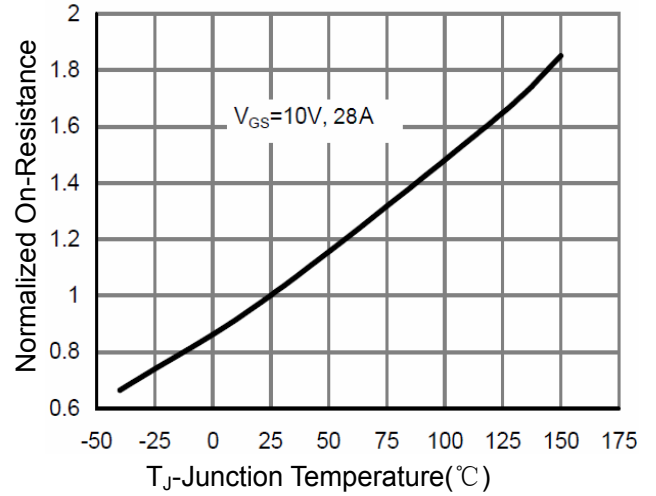


Figure 4 Rdson-Junction Temperature

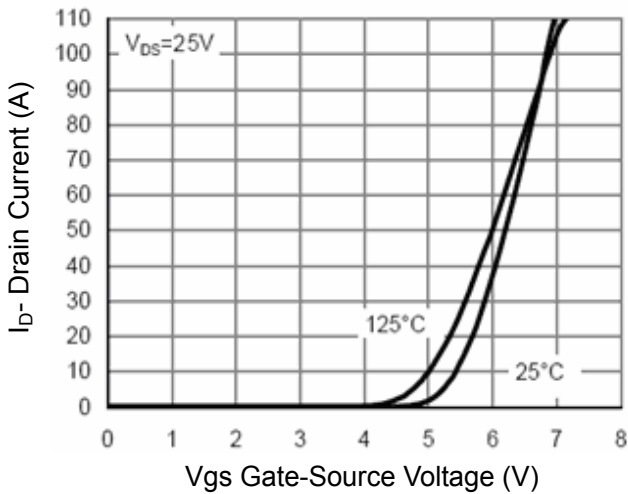


Figure 2 Transfer Characteristics

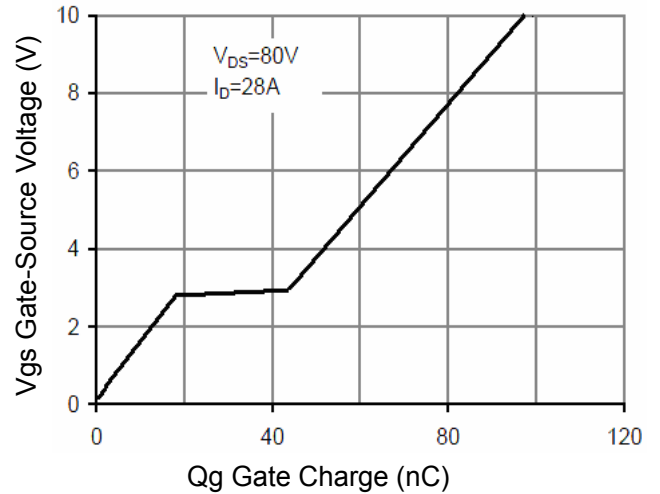


Figure 5 Gate Charge

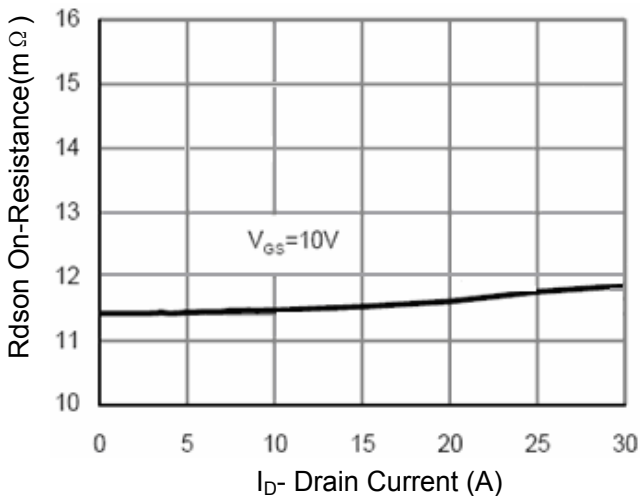


Figure 3 Rdson- Drain Current

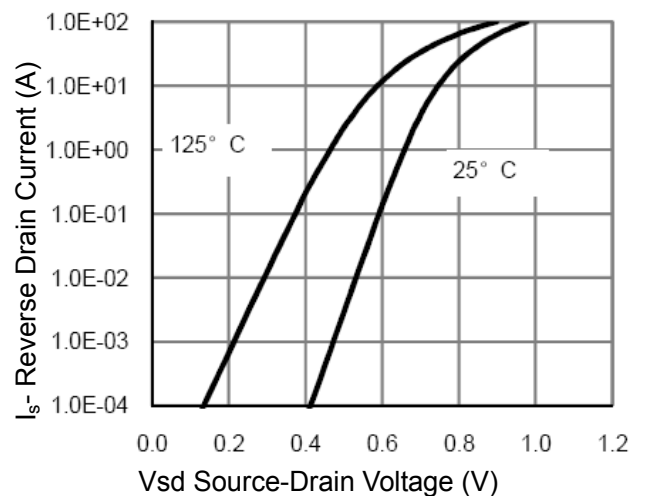


Figure 6 Source- Drain Diode Forward

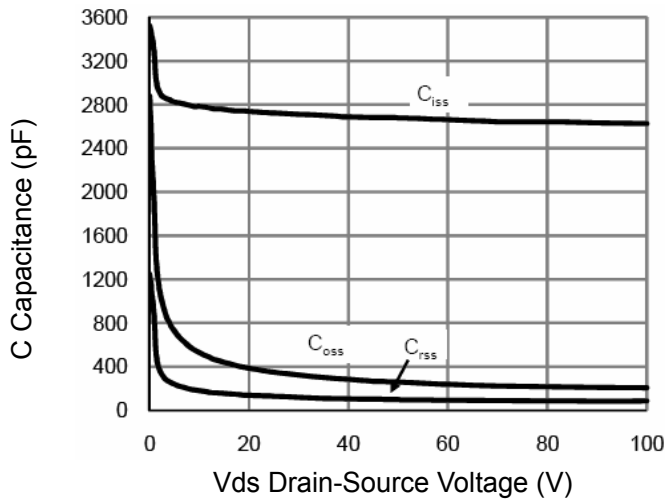


Figure 7 Capacitance vs Vds

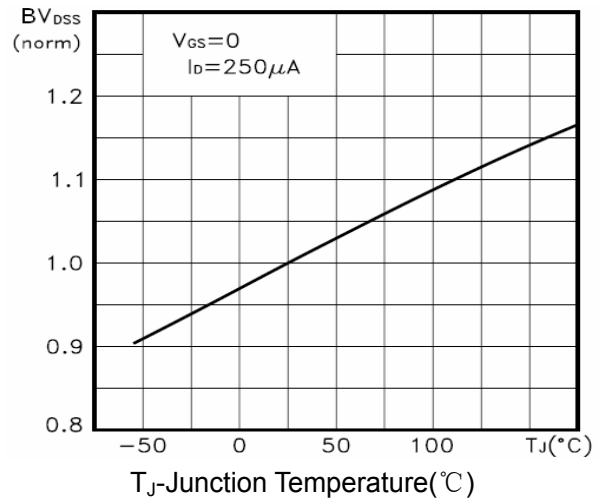


Figure 9 BV_{DSS} vs Junction Temperature

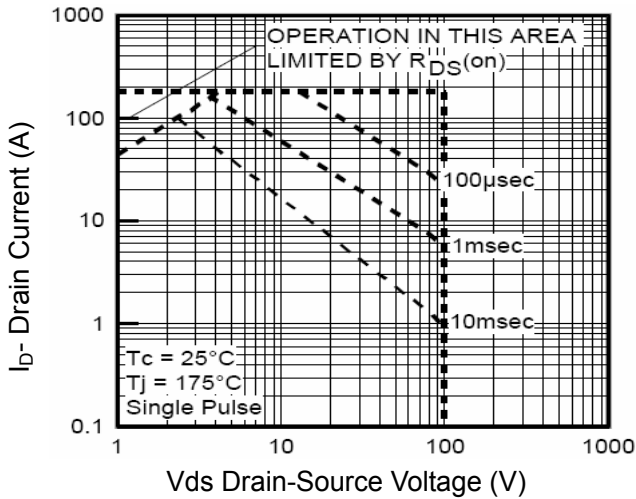


Figure 8 Safe Operation Area

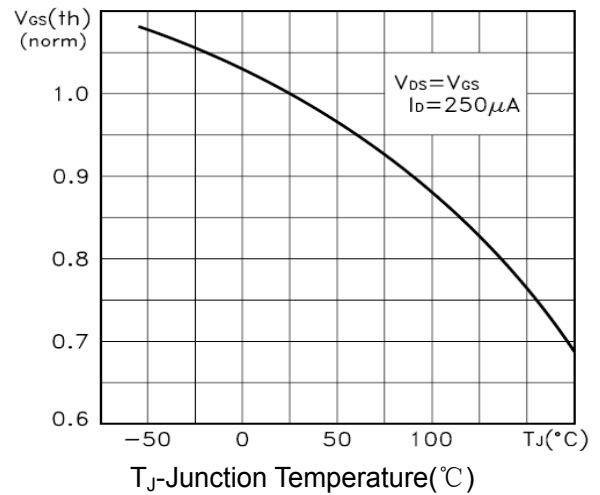


Figure 10 $V_{GS(th)}$ vs Junction Temperature

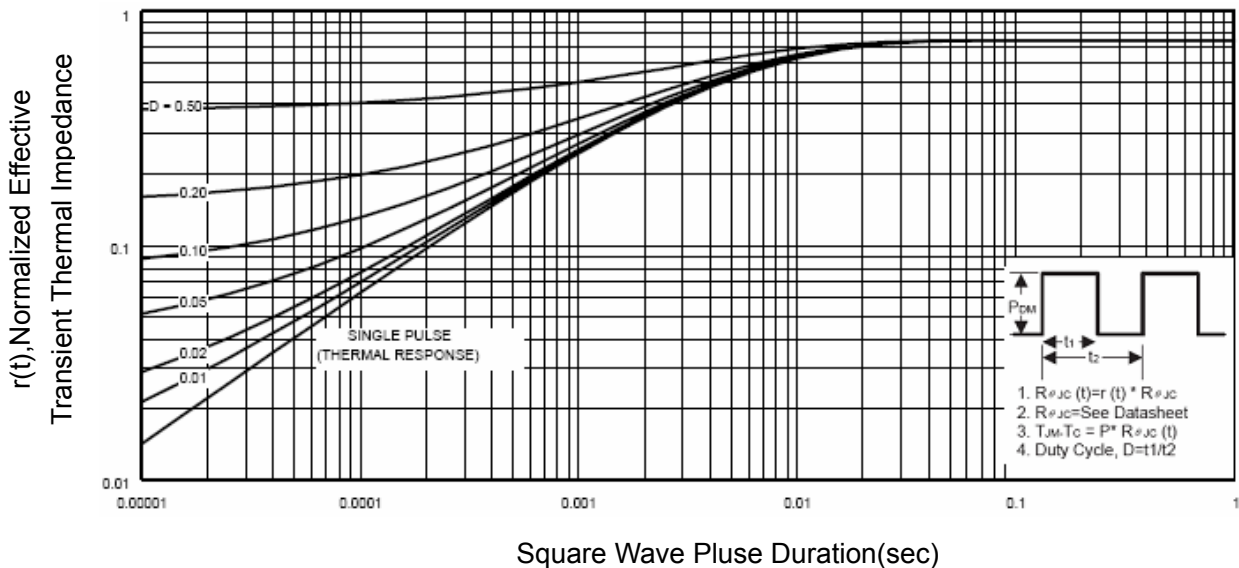
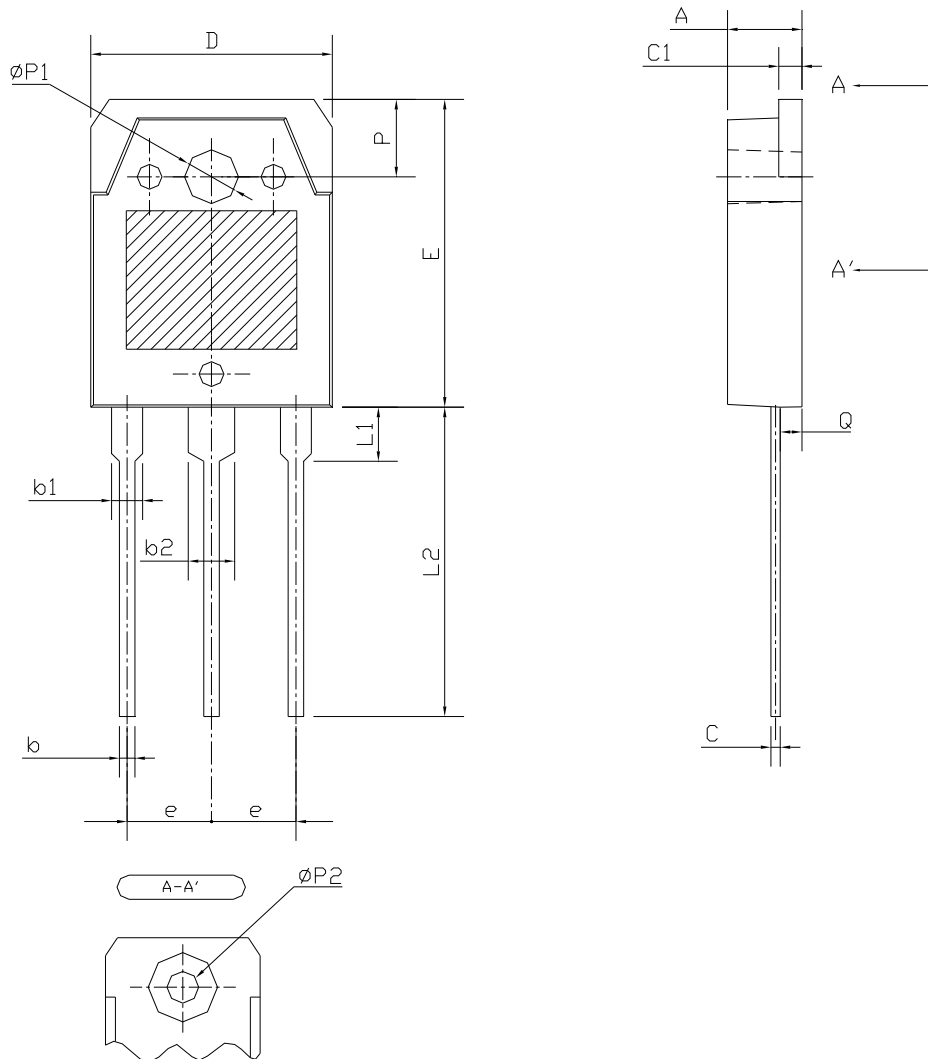


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Outline Dimensions


SYMBOL	MIN	NOM	MAX
A	4.60	4.80	5.00
b	0.80	1.00	1.20
b1	1.80	2.00	2.20
b2	2.80	3.00	3.20
C	0.55	0.60	0.75
C1	1.45	1.50	1.65
D	15.40	15.60	15.80
E	19.70	19.90	20.10
e	5.15	5.45	5.75
L1	3.30	3.50	3.70
L2	19.80	20.00	20.20
P	4.80	5.00	5.20
$\phi P1$	3.30	3.40	3.50
$\phi P2$	(3.20)		
Q	1.20	1.40	1.60