N-Channel Enhancement Mode Power Mosfet

Description

The FIR60N20AN uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

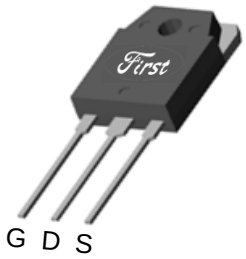
General Features

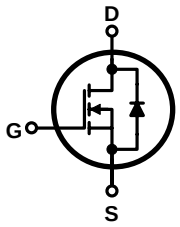
- V_{DS} =200V,I_D =60A
  $R_{DS(ON)}$ <32mΩ @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

PIN Connection TO-3P





Marking Diagram

Y	= Year
A	= Assembly Location
WW	= Work Week
FIR60N20AN	= Specific Device Code

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR60N20AN	FIR60N20ANG	TO-3P	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	60	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	42	A
Pulsed Drain Current	I_{DM}	280	A
Maximum Power Dissipation	P_D	300	W
Derating factor		2.0	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	506	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.5	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

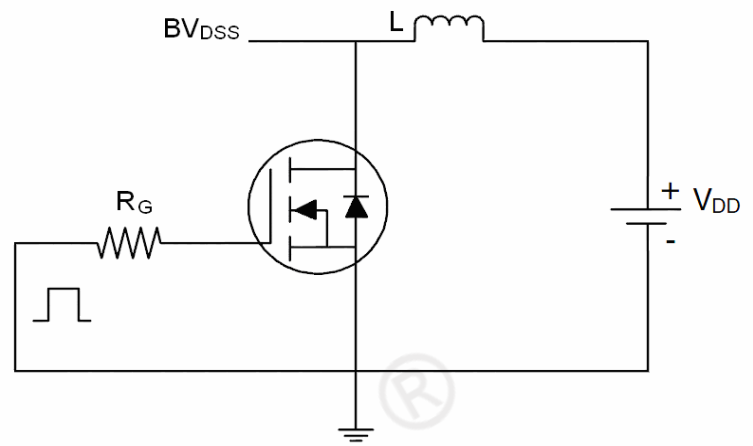
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	200	220	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3.2	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	24	32	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=30A	40	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	6200	-	PF
Output Capacitance	C_{oss}		-	950	-	PF
Reverse Transfer Capacitance	C_{rss}		-	460	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=100V, R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	33	-	nS
Turn-on Rise Time	t_r		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	21	-	nS
Turn-Off Fall Time	t_f		-	31	-	nS
Total Gate Charge	Q_g	V_{DS}=100V,I_D=30A, V_{GS}=10V	-	130		nC
Gate-Source Charge	Q_{gs}		-	36		nC
Gate-Drain Charge	Q_{gd}		-	46		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=30A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	60	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 30A di/dt = 100A/μs (Note3)	-	42		nS
Reverse Recovery Charge	Qrr		-	66		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

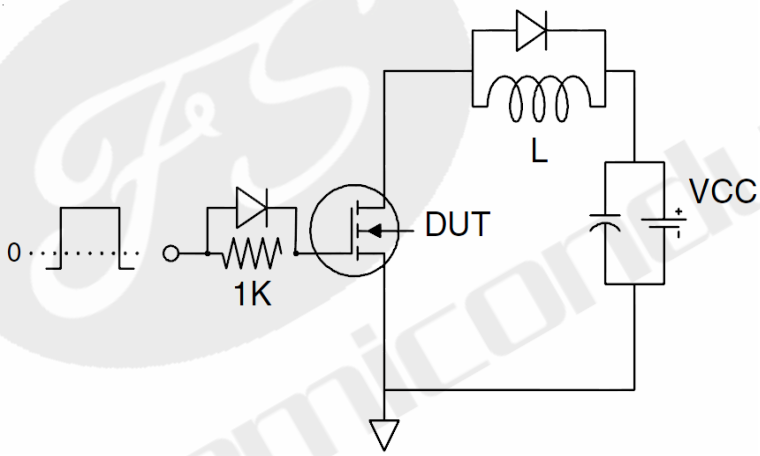
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: j=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

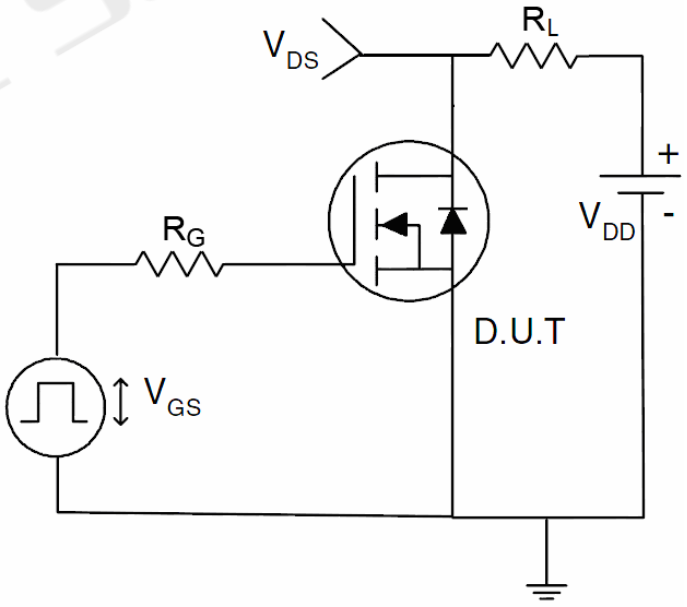
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

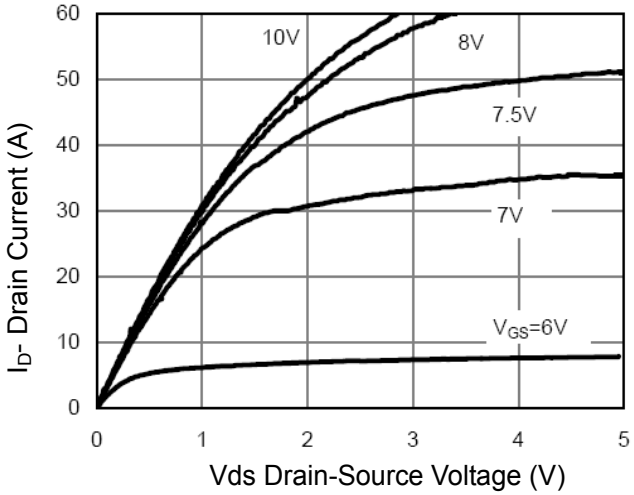


Figure 1 Output Characteristics

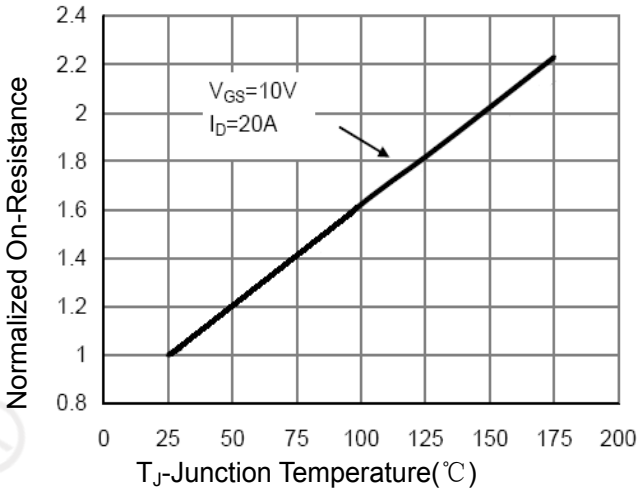


Figure 4 Rdson-Junction Temperature

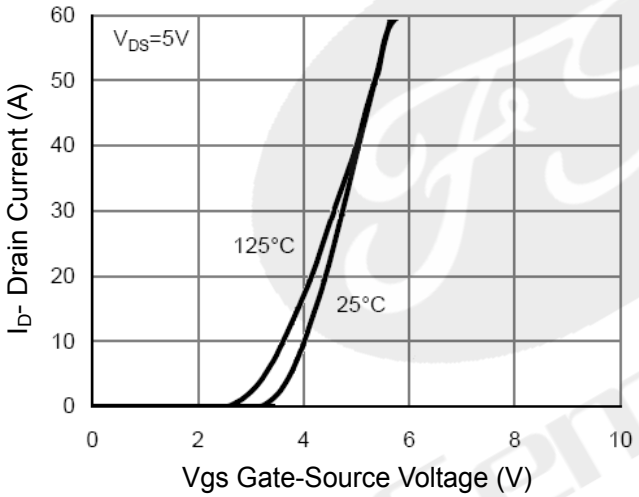


Figure 2 Transfer Characteristics

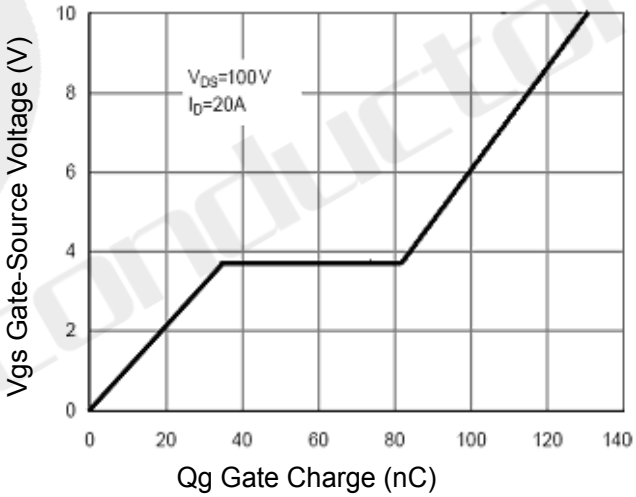


Figure 5 Gate Charge

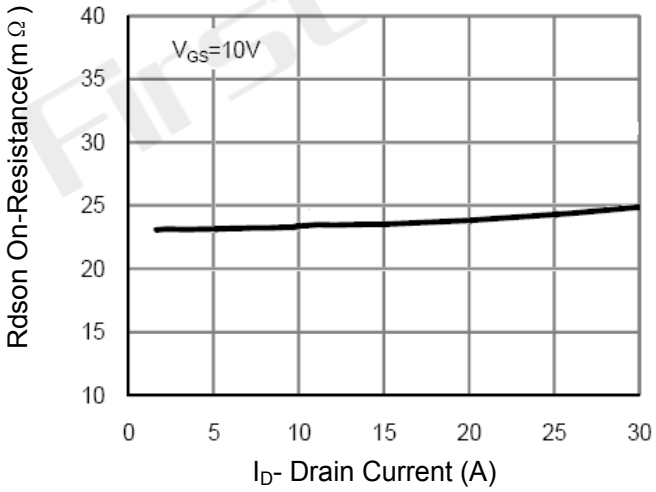


Figure 3 Rdson- Drain Current

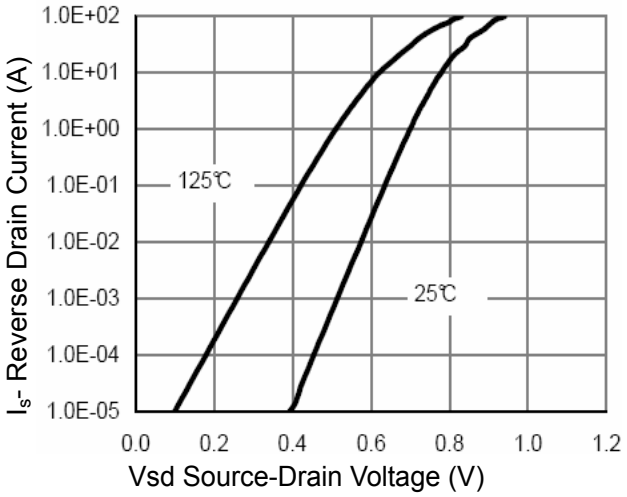


Figure 6 Source- Drain Diode Forward

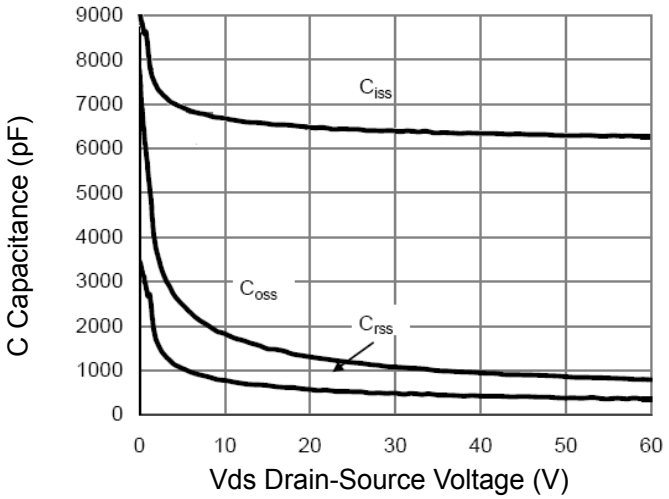


Figure 7 Capacitance vs Vds

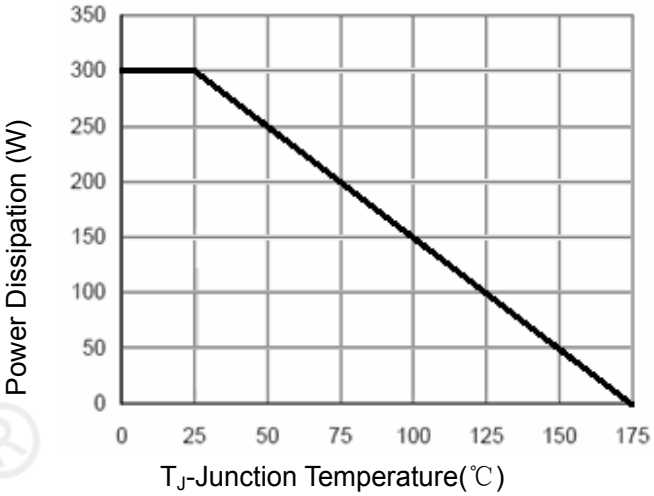


Figure 9 Power De-rating

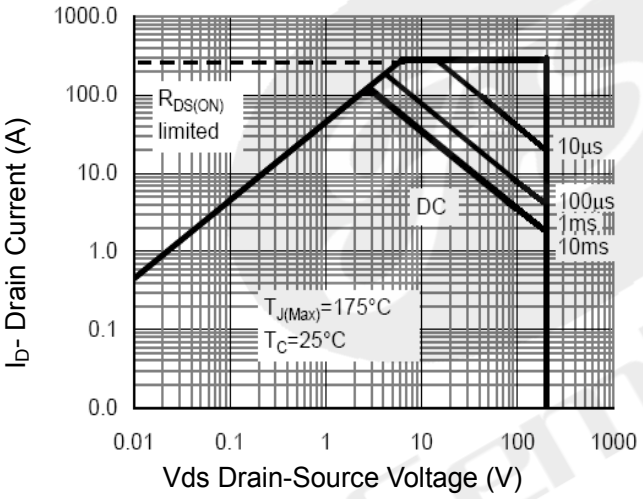


Figure 8 Safe Operation Area

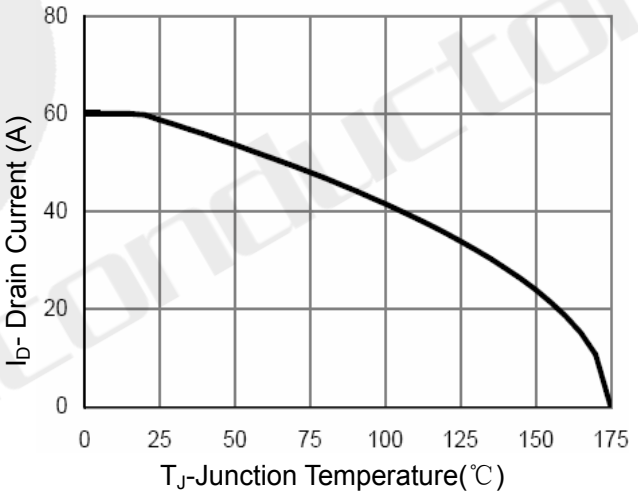


Figure 10 Current De-rating

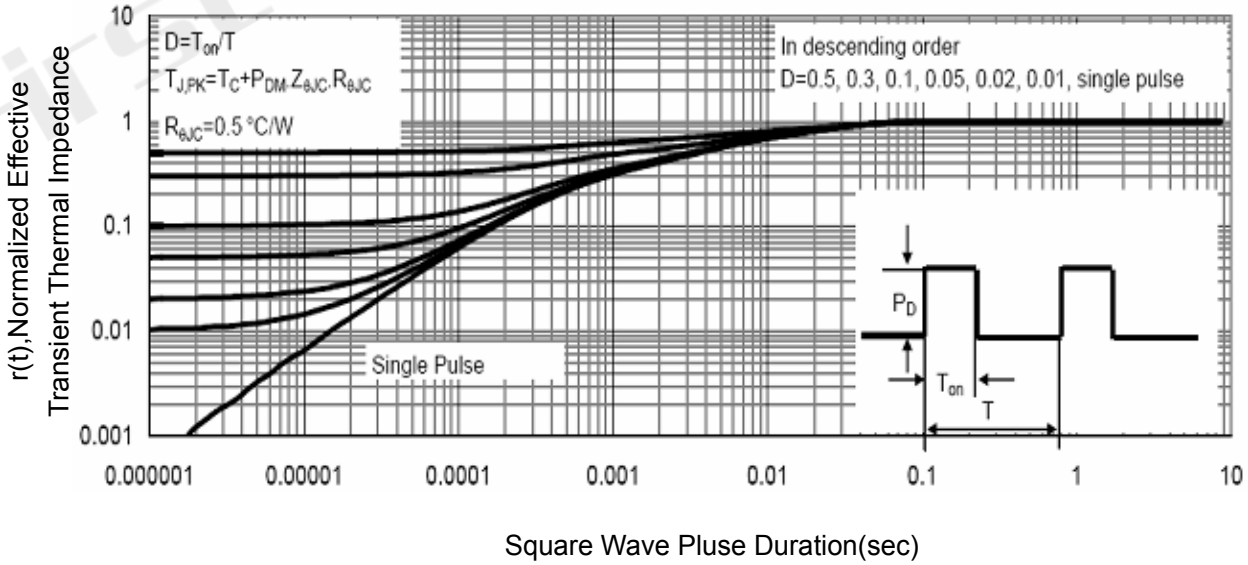
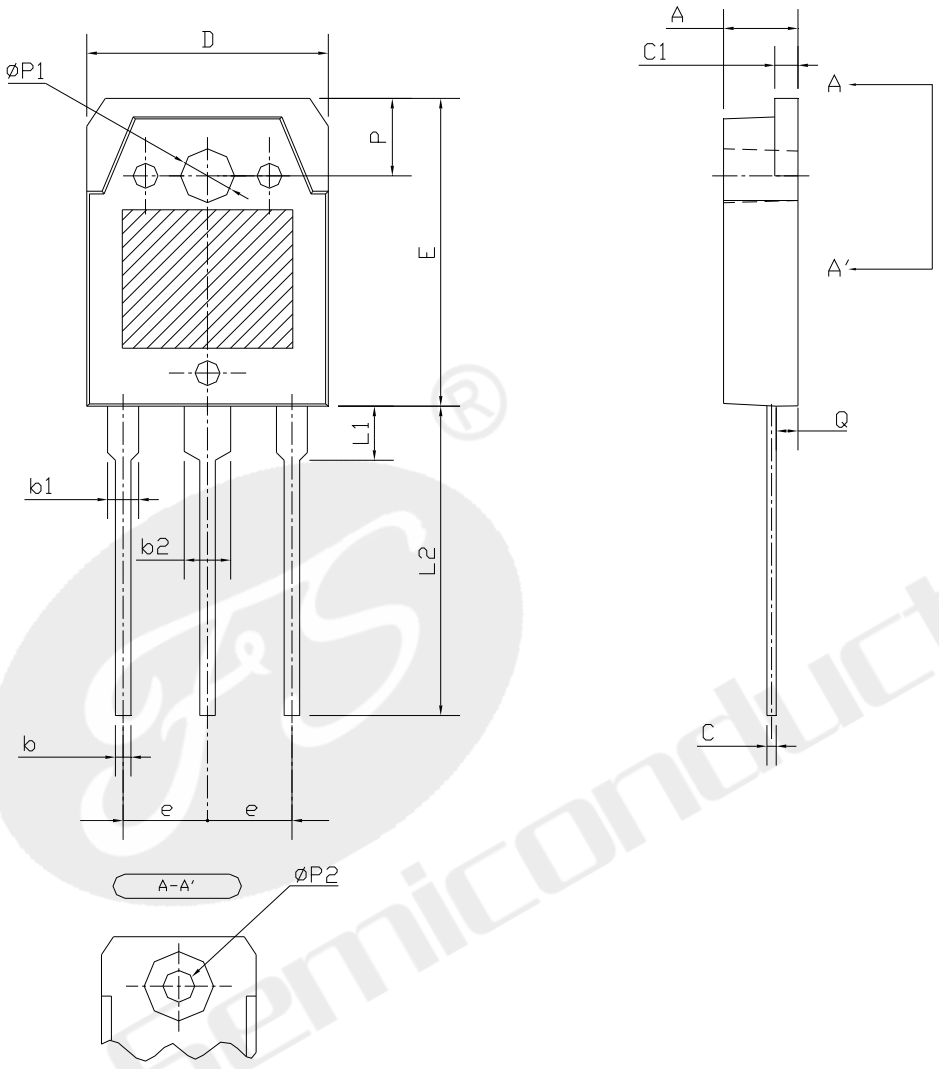


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Outline Dimensions



SYMBOL	MIN	NOM	MAX
A	4.60	4.80	5.00
b	0.80	1.00	1.20
b1	1.80	2.00	2.20
b2	2.80	3.00	3.20
C	0.55	0.60	0.75
C1	1.45	1.50	1.65
D	15.40	15.60	15.80
E	19.70	19.90	20.10
e	5.15	5.45	5.75
L1	3.30	3.50	3.70
L2	19.80	20.00	20.20
P	4.80	5.00	5.20
ØP1	3.30	3.40	3.50
ØP2		(3.20)	
Q	1.20	1.40	1.60

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	