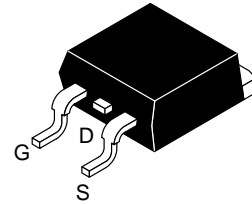




PIN Connection TO-263-2L

DESCRIPTION

The FIR110N08RG uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

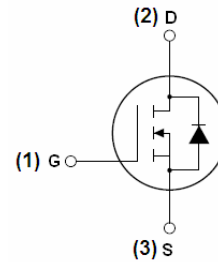


GENERAL FEATURES

- $V_{DS} = 80V, I_D = 105A$   
 $R_{DS(ON)} < 8m\Omega @ V_{GS} = 10V$  (Typ: 6.3m $\Omega$ )
- High density cell design for ultra low  $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Marking Diagram

- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR110N08R = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR110N08R	FIR110N08RG	TO-263-2L	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	105	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	80	A
Pulsed Drain Current	$I_{DM}$	420	A
Maximum Power Dissipation	$P_D$	200	W
Derating factor		1.33	W/°C
Single pulse avalanche energy (Note 5)	$E_{AS}$	800	mJ



Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	°C
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**Thermal Characteristic**

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.75	°C/W
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**Electrical Characteristics (TA=25°C unless otherwise noted)**

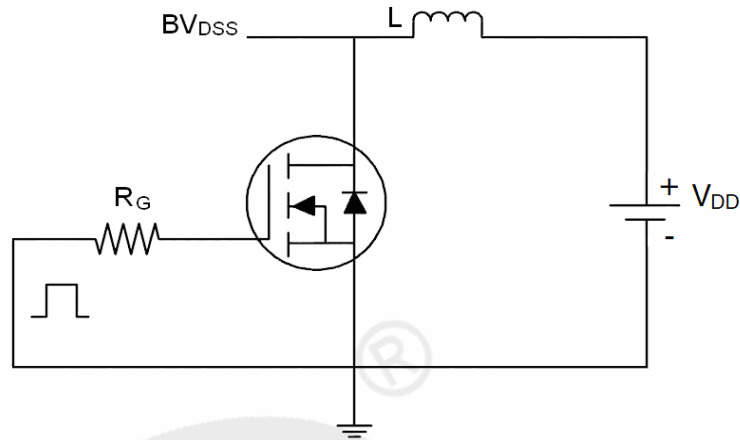
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	80	86	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	6.3	8	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=25V, I_D=40A$	80	-	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	4900	-	PF
Output Capacitance	$C_{OSS}$		-	410	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	315	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega,$ $R_G=2.5\Omega, V_{GS}=10V$	-	20	-	nS
Turn-on Rise Time	$t_r$		-	19	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	$t_f$		-	30	-	nS
Total Gate Charge	$Q_g$	$I_D=30A, V_{DD}=30V, V_{GS}=10V$	-	125	-	nC
Gate-Source Charge	$Q_{GS}$		-	24	-	nC
Gate-Drain Charge	$Q_{gd}$		-	49	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	105	A
Reverse Recovery Time	$t_{rr}$	$T_J=25^\circ C, I_F=75A,$ $di/dt=100A/\mu S$ (Note 3)	-	37		nS
Reverse Recovery Charge	$Q_{rr}$		-	58		nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

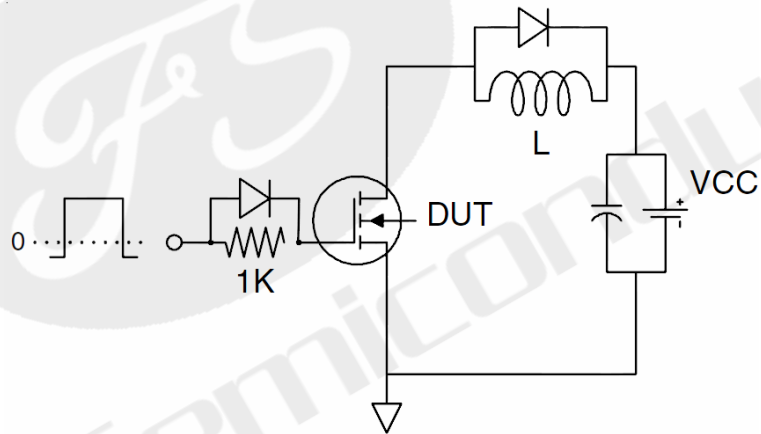
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ C, V_{DD}=40V, V_G=10V, L=0.5mH, R_g=25\Omega$

## Test circuit

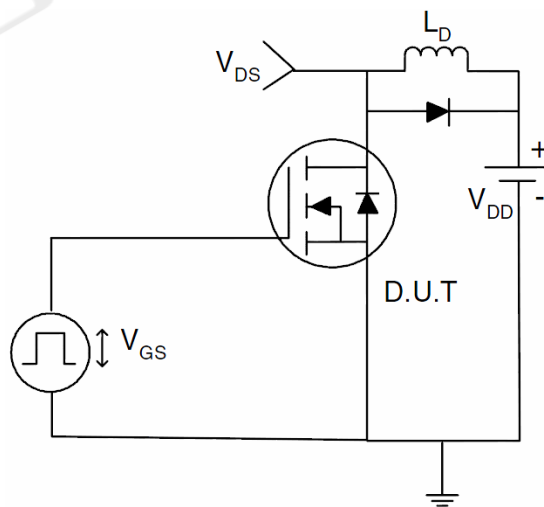
### 1) $E_{AS}$ test Circuits



### 2) Gate charge test Circuit:



### 3) Switch Time Test Circuit:





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

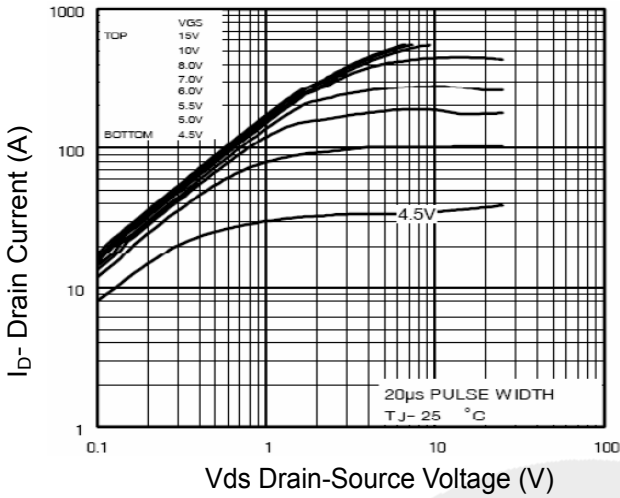


Figure 1 Output Characteristics

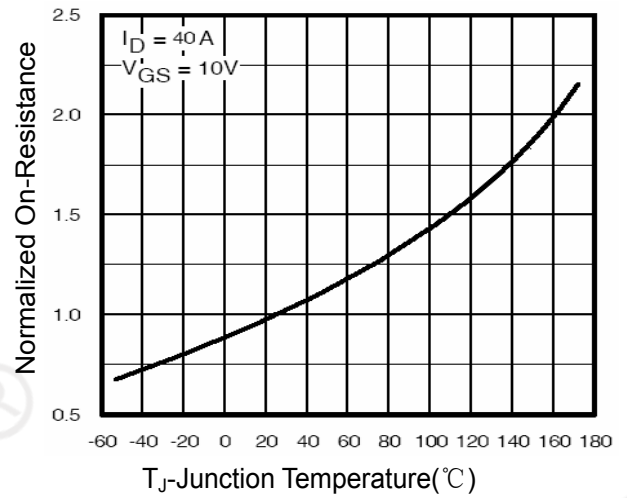


Figure 4 Rdson-Junction Temperature

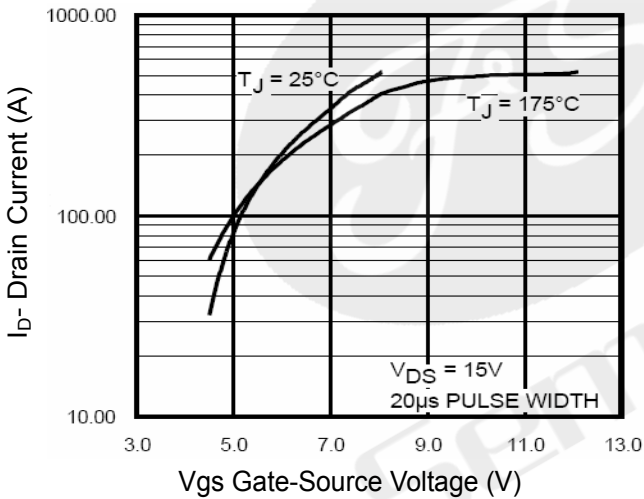


Figure 2 Transfer Characteristics

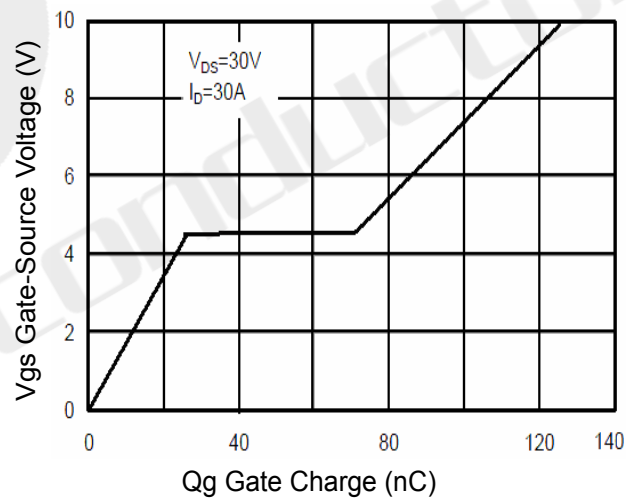


Figure 5 Gate Charge

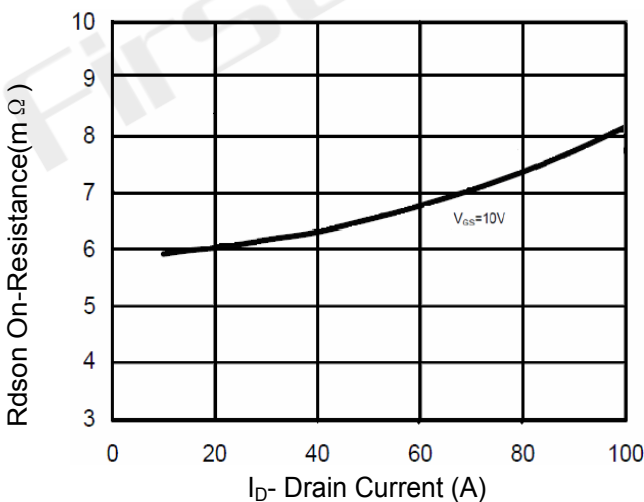


Figure 3 Rdson- Drain Current

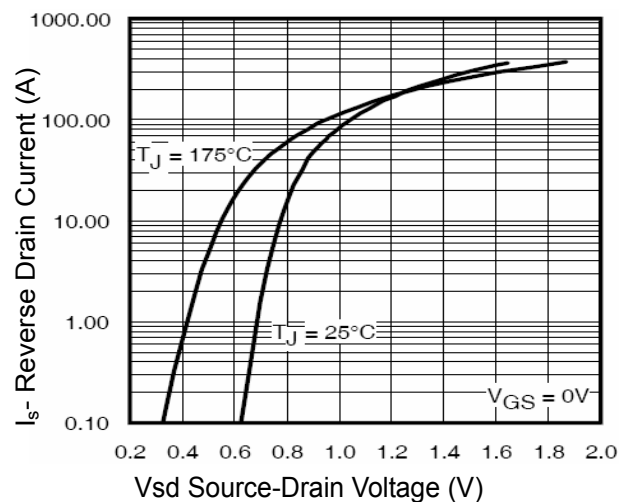


Figure 6 Source- Drain Diode Forward

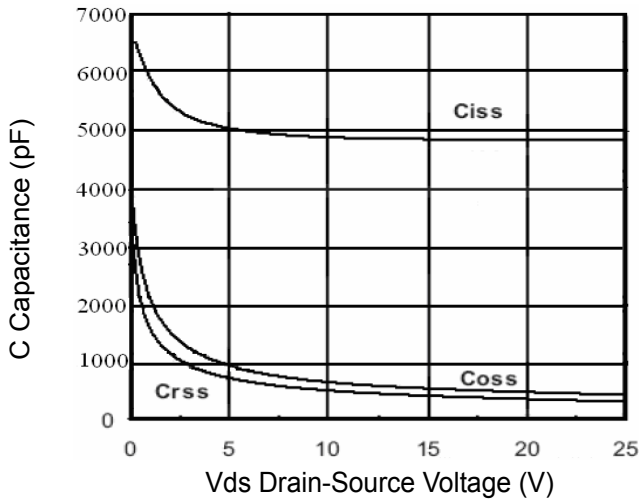


Figure 7 Capacitance vs Vds

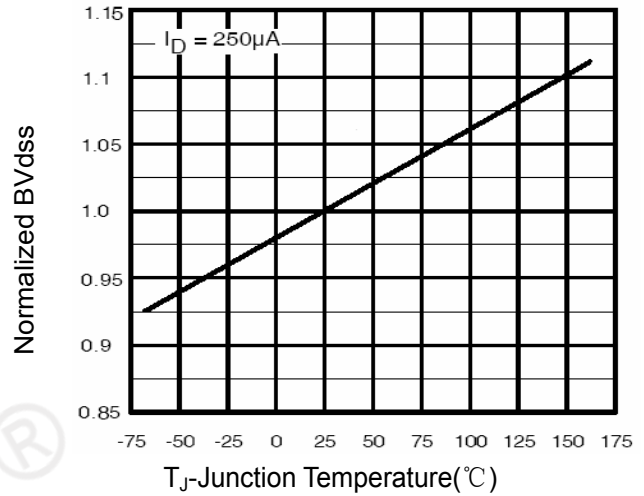


Figure 9  $BV_{DSS}$  vs Junction Temperature

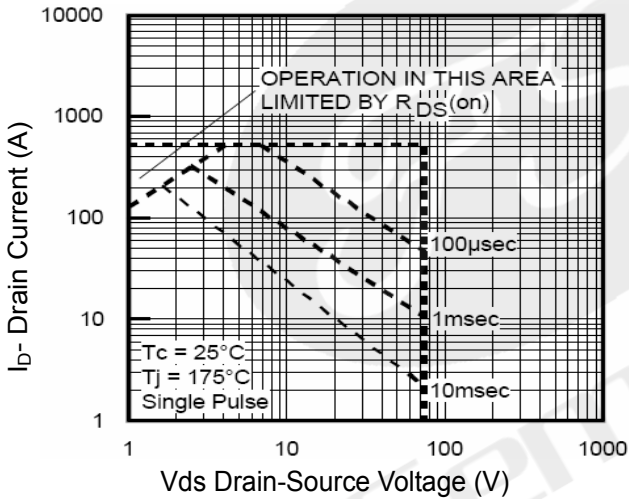


Figure 8 Safe Operation Area

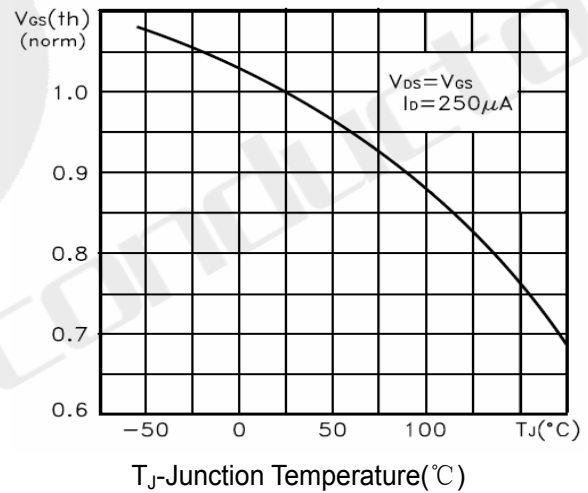


Figure 10  $V_{GS(th)}$  vs Junction Temperature

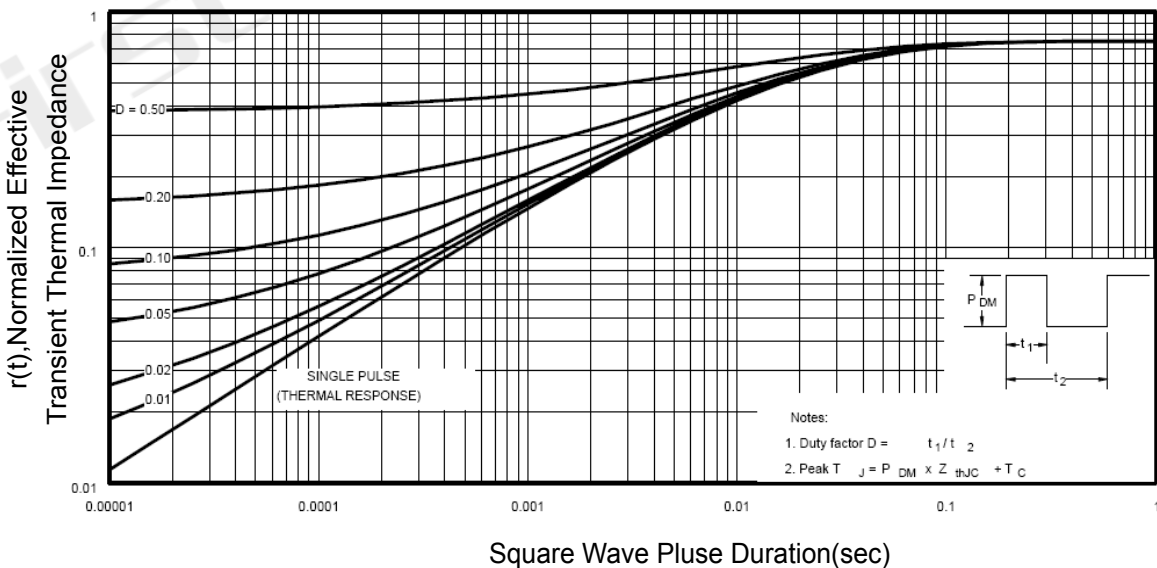
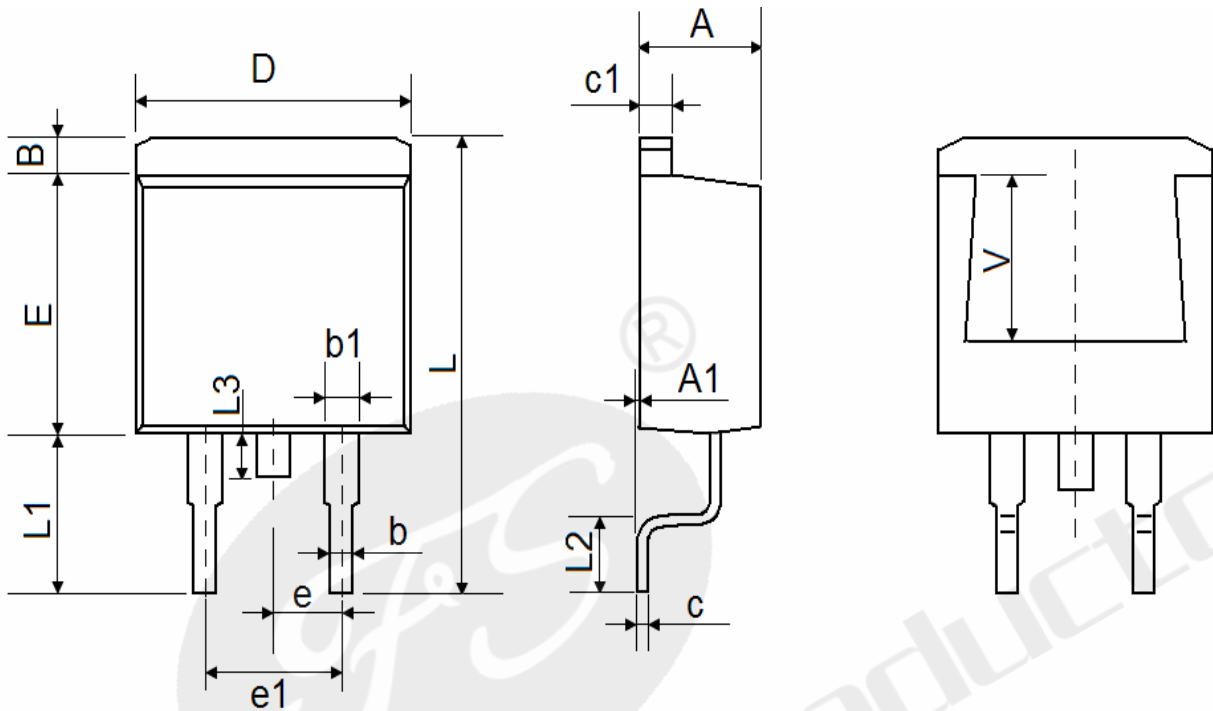


Figure 11 Normalized Maximum Transient Thermal Impedance

## Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF		0.220 REF	



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

**ATTACHMENT**

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	