First Semiconductor

FIR24N60ANG

N-Channel Power MOSFET

FERTURES

- TYPICAL R_{DS}(on) = 0.19Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

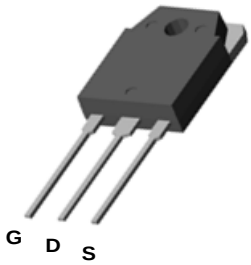
DESCRIPTION

This improved version of MDmesh™ which is based on Multiple Drain process represents the new bench-mark in high voltage MOSFETs. The resulting product exhibits even lower on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall performances that are significantly better than that of similar competition's products.

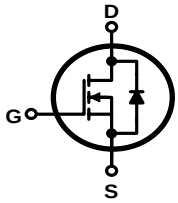
APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing sys-tem miniaturization and higher efficiencies.

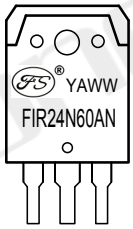
PIN Connection TO-3P



Schematic diagram



Marking Diagram



Y	= Year
A	= Assembly Location
WW	= Work Week
FIR24N60AN	= Specific Device Code

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuous) at T_C = 25°C	24	A
I_D	Drain Current (continuous) at T_C = 100°C	12.6	A
I_{DM} (•)	Drain Current (pulsed)	80	A
P_{TOT}	Total Dissipation at T_C = 25°C	192	W
dv/dt(1)	Peak Diode Recovery voltage slope	15	V/ns
V_{ISO}	Insulation Winthstand Voltage (DC)	2500	V
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area; (*)Limited only by maximum temperature allowed

(1) I_{SD} ≤24A, di/dt ≤400A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

THERMAL DATA

Symbol	Parameter	Value	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.65	W/°C
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	12	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	650	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 12 A		0.19	0.25	Ω

ELECTRICAL CHARACTERISTICS (CONTINUE)
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 12 A		TBD		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1590 803 52		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		130		pF
R_g	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 200 V, I_D = 12 A R_G = 4.7Ω V_{GS} = 10 V (see test circuit, Figure 3)		25 20		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V, I_D = 24 A, V_{GS} = 10 V		40 11 25	71	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 480 V, I_D = 24 A, R_G = 4.7Ω, V_{GS} = 10 V (see test circuit, Figure 5)		13		ns
t_f	Fall Time			15		ns
t_c	Cross-over Time			26		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
I_{SDM} (2)	Source-drain Current (pulsed)				80	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 24 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} =24A,di/dt=100A/µs, V_{DD} = 100 V, T_j = 25°C (see test circuit, Figure 5)		416 5.6 27		ns µC A
t_{rr} Q_{rr} I_{rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} =24A,di/dt=100A/µs, V_{DD} = 100 V, T_j = 150°C (see test circuit, Figure 5)		544 7.3 28		ns µC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

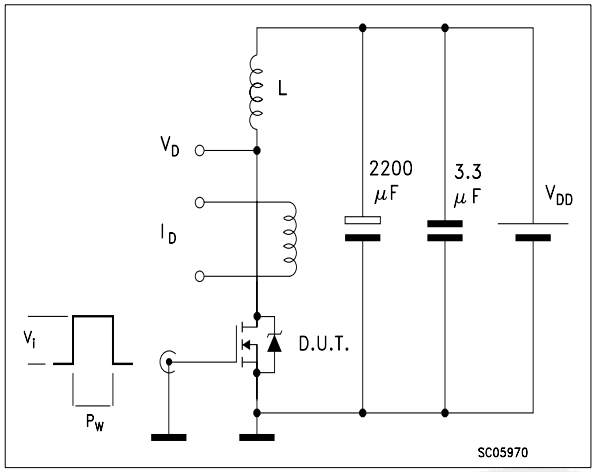


Fig. 2: Unclamped Inductive Waveform

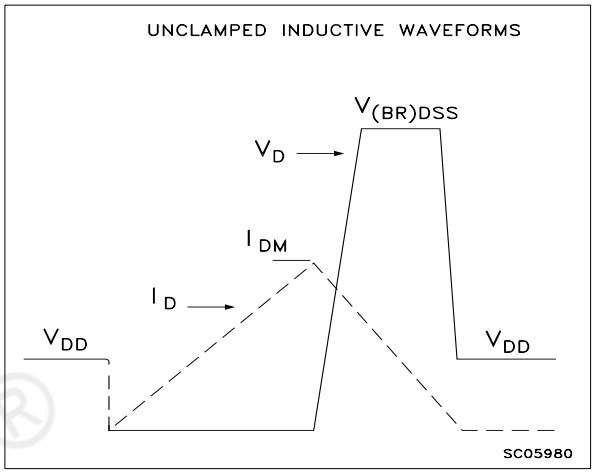


Fig. 3: Switching Times Test Circuit For Resistive Load

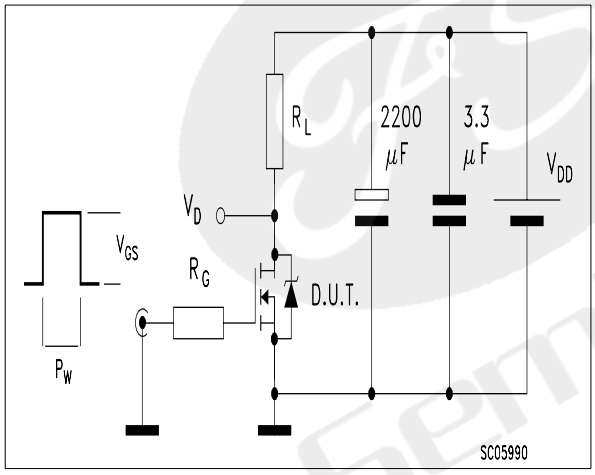


Fig. 4: Gate Charge test Circuit

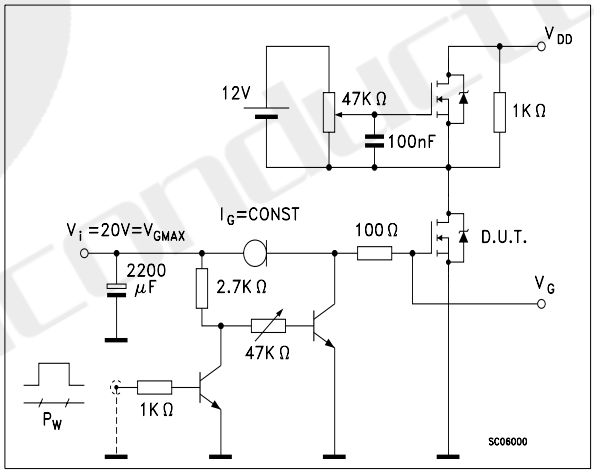
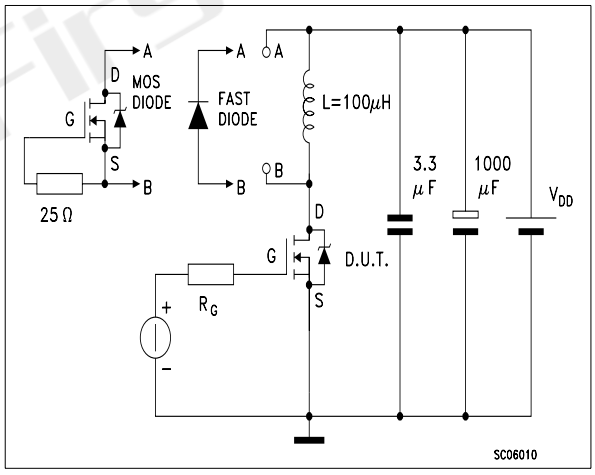
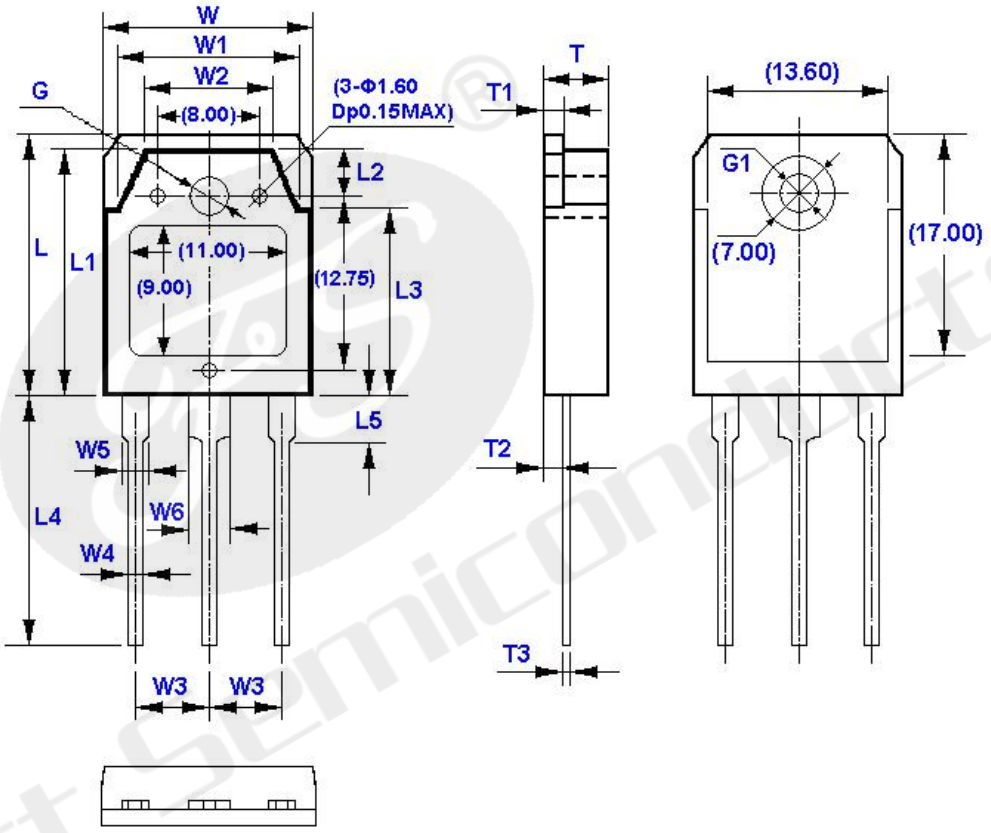


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Package Outline Dimensions TO-3P

Units: mm



符号	尺寸		符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max		Min	Max
W	15.40	15.80	W5	1.80	2.20	L3	13.70	14.10	T2	1.20	1.60
W1	13.40	13.80	W6	2.80	3.20	L4	19.70	20.30	T3	0.55	0.75
W2	9.40	9.80	L	19.70	20.10	L5	3.30	3.70	G (Φ) (正面)	3.30	3.50
W3	5.45 (TYP)		L1	18.50	18.90	T	4.60	5.00	G1(Φ) (背面)	3.10	3.30
W4	0.80	1.20	L2	3.60	4.00	T1	1.45	1.65			

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	