



Description

The FIR110N15ANG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

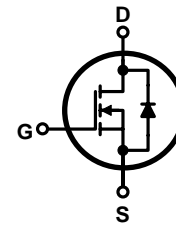
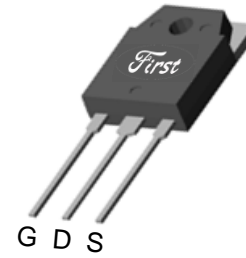
General Features

- $V_{DSS} = 150V, I_D = 110A$
 $R_{DS(ON)} < 13m\Omega @ V_{GS}=10V$ (Typ: 10 m Ω)
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Automotive applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

PIN Connection TO-3P



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR110N15AN = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR110N15AN	FIR110N15ANG	TO-3P	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	110	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	80	A
Pulsed Drain Current	I_{DM}	390	A
Maximum Power Dissipation	P_D	385	W
Derating factor		2.57	W/°C
Single pulse avalanche energy (Note 3)	E_{AS}	1800	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	3	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	0.39	$^{\circ}C/W$
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Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

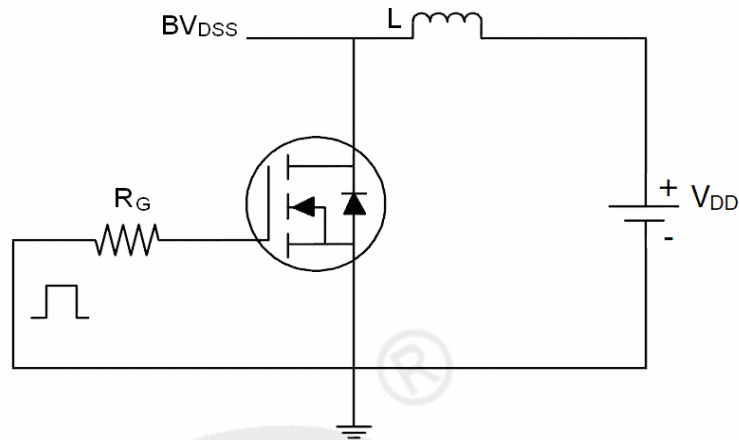
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	150	160	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=150V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	10	13	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=50V, I_D=40A$	50	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	16500	-	PF
Output Capacitance	C_{OSS}		-	1344	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	1025	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$ (Note2)	-	20	-	nS
Turn-on Rise Time	t_r		-	130	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	t_f		-	60	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$ (Note2)	-	377	-	nC
Gate-Source Charge	Q_{gs}		-	79	-	nC
Gate-Drain Charge	Q_{gd}		-	118	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}C, I_F=40A$	-	60	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$ (Note2)	-	90	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

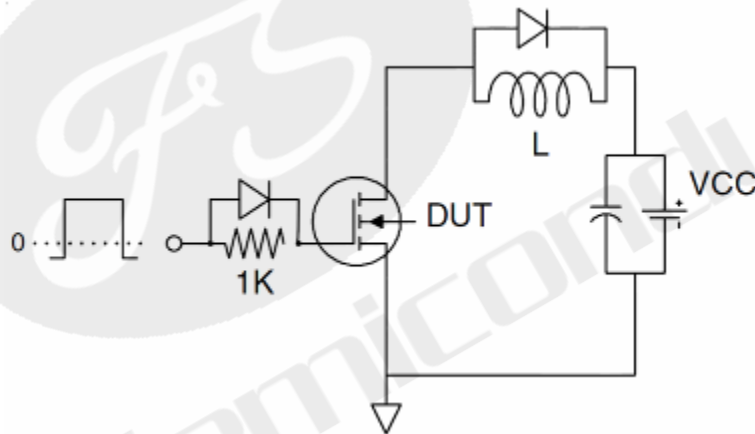
1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
3. EAS condition: $T_J=25^{\circ}C, V_{DD}=75V, V_G=10V, L=2mH, R_G=25\Omega$
4. $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^{\circ}C$

Test circuit

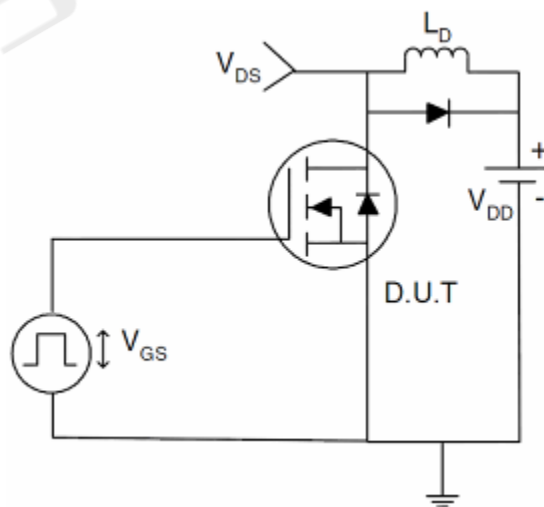
1) E_{AS} test Circuits



2) Gate charge test Circuit:

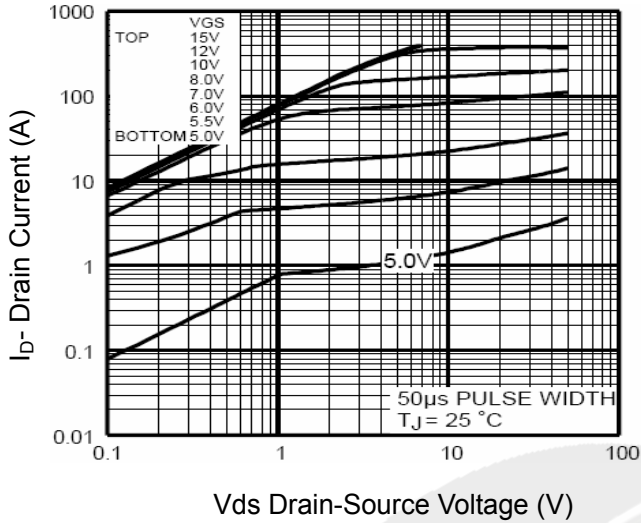


3) Switch Time Test Circuit:

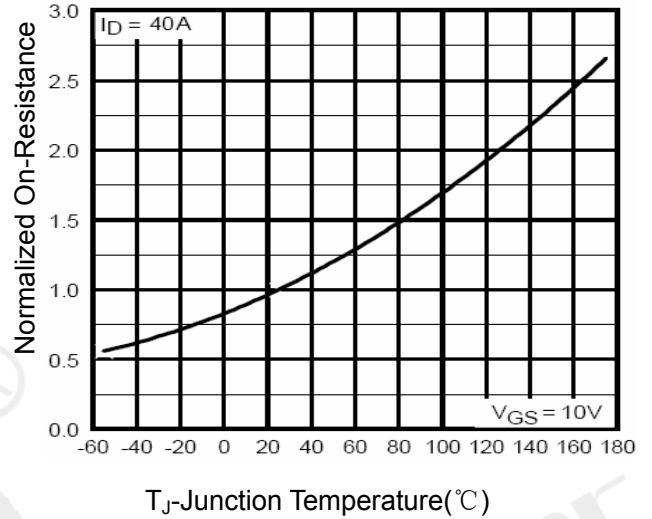




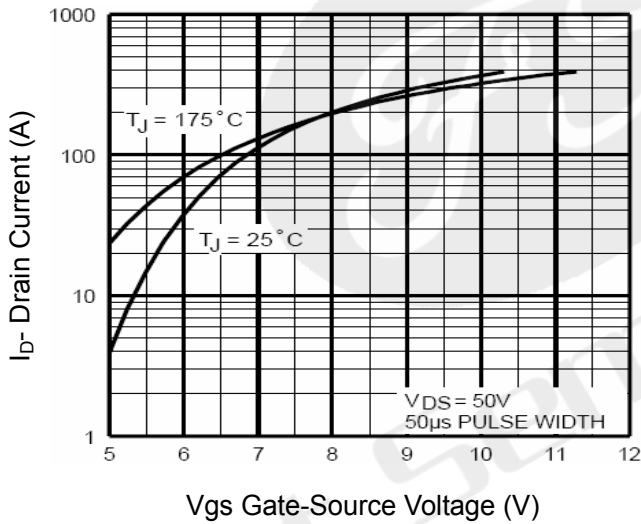
Typical Electrical And Thermal Characteristics(Curves)



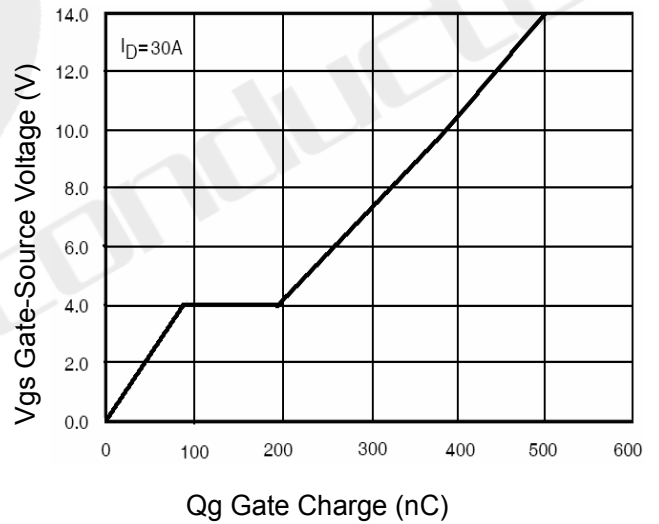
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



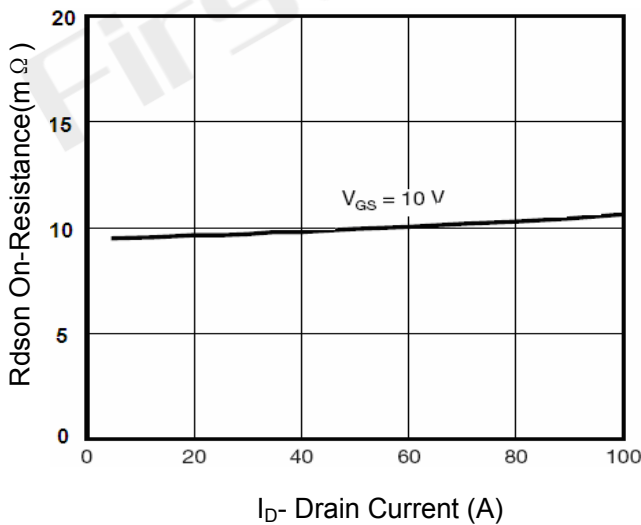
T_J -Junction Temperature($^\circ\text{C}$)
Figure 4 Rdson-Junction Temperature



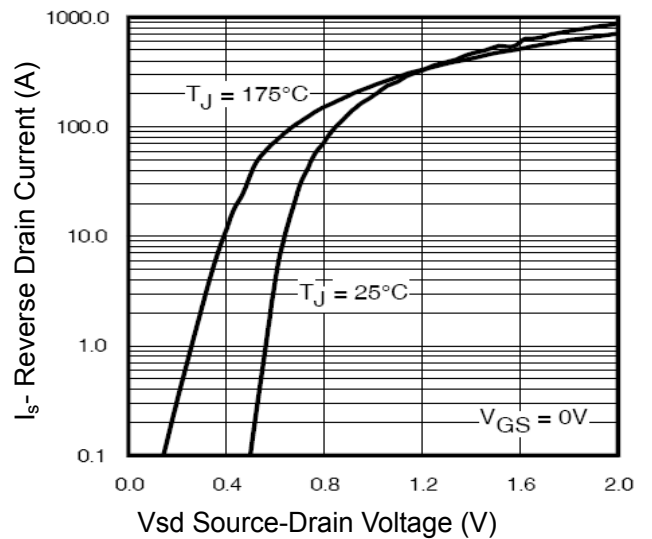
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



Qg Gate Charge (nC)
Figure 5 Gate Charge



I_D - Drain Current (A)
Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward

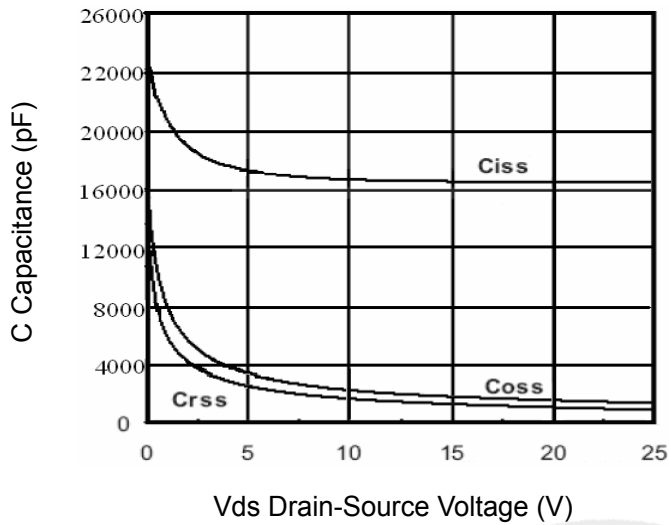


Figure 7 Capacitance vs Vds

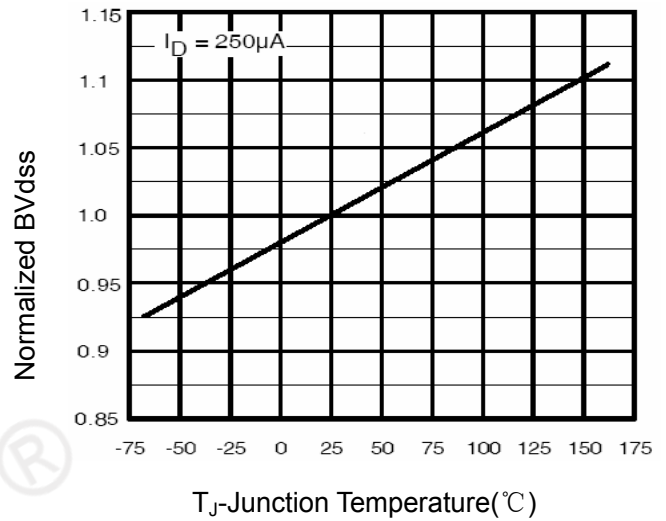


Figure 9 BV_{DSS} vs Junction Temperature

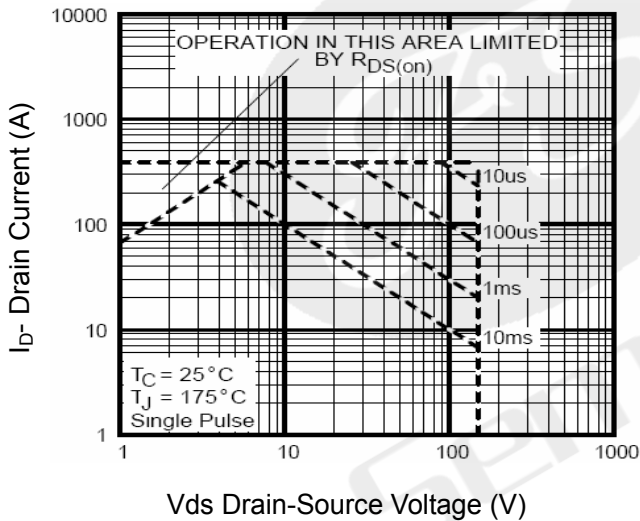


Figure 8 Safe Operation Area

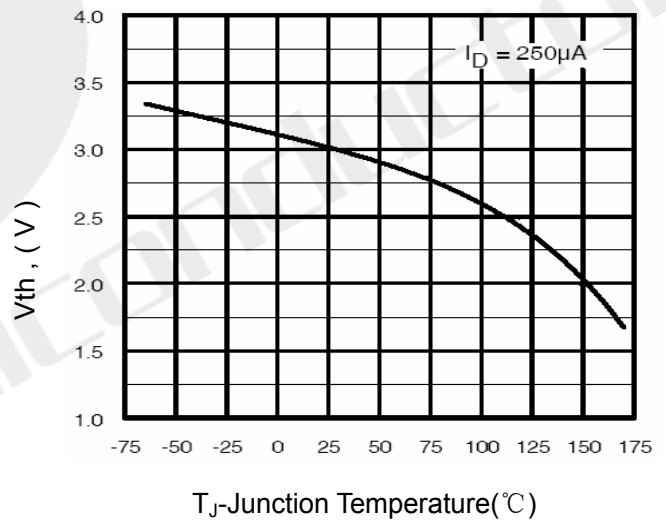


Figure 10 V_{GS(th)} vs Junction Temperature

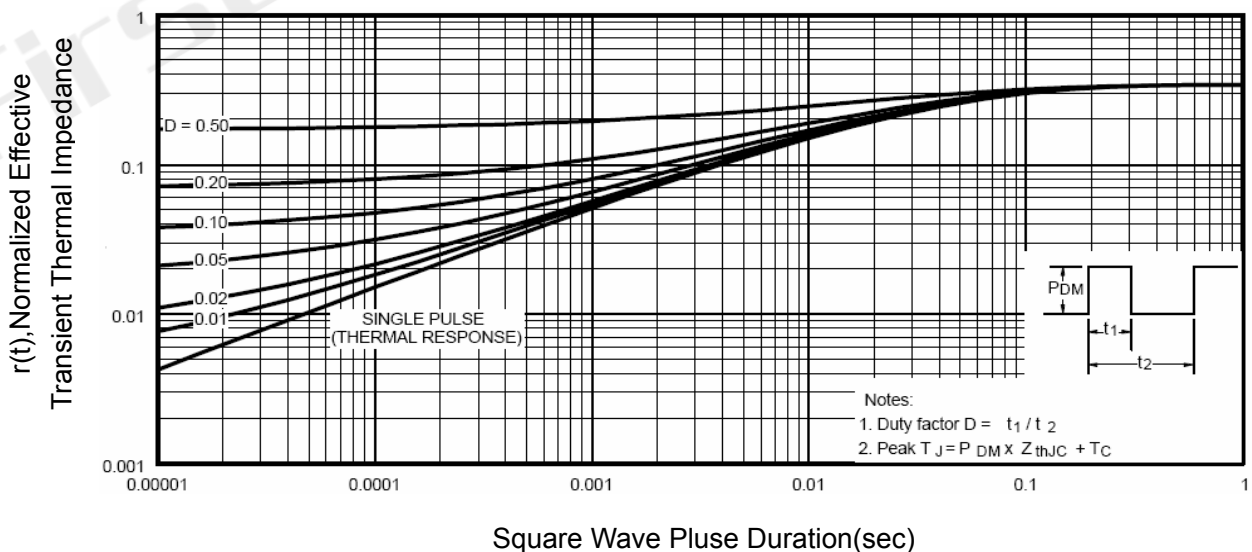
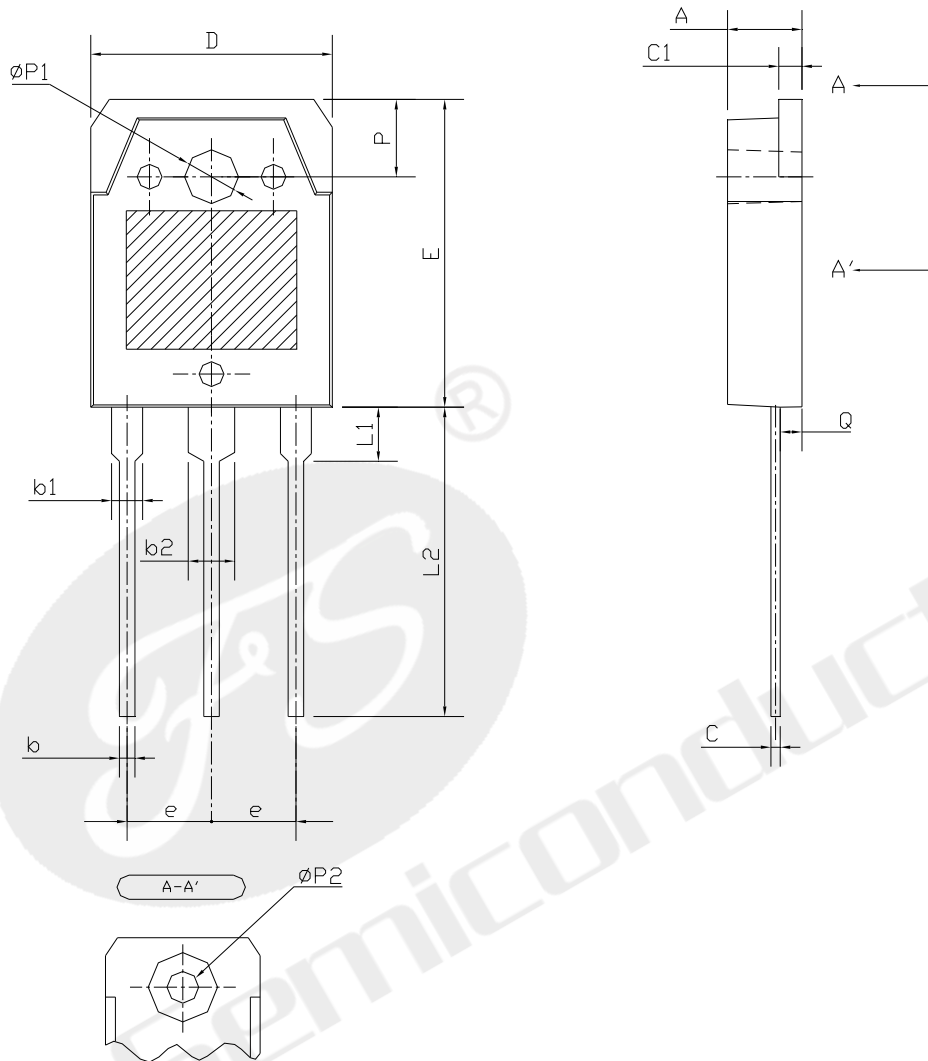


Figure 11 Normalized Maximum Transient Thermal Impedance



Package Outline Dimensions



SYMBOL	MIN	NOM	MAX
A	4.60	4.80	5.00
b	0.80	1.00	1.20
b1	1.80	2.00	2.20
b2	2.80	3.00	3.20
C	0.55	0.60	0.75
C1	1.45	1.50	1.65
D	15.40	15.60	15.80
E	19.70	19.90	20.10
e	5.15	5.45	5.75
L1	3.30	3.50	3.70
L2	19.80	20.00	20.20
P	4.80	5.00	5.20
ØP1	3.30	3.40	3.50
ØP2	(3.20)		
Q	1.20	1.40	1.60



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	

