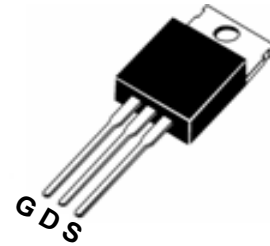




PIN Connection TO-220AB

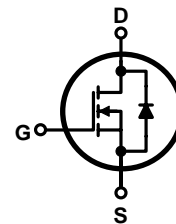


Description

The FIR210N075PG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

General Features

- $V_{DSS} = 75V, I_D = 210A$ (Note5)
 $R_{DS(ON)} < 4.5m\Omega @ V_{GS} = 10V$
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Excellent package for good heat dissipation



Application

- Automotive applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR210N075P = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR210N075P	FIR210N075PG	TO-220	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	75	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	210 (Note5)	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	150	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/°C
Single pulse avalanche energy (Note 3)	E_{AS}	2200	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	0.48	$^{\circ}\text{C/W}$
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Electrical Characteristics (TA=25°C unless otherwise noted)

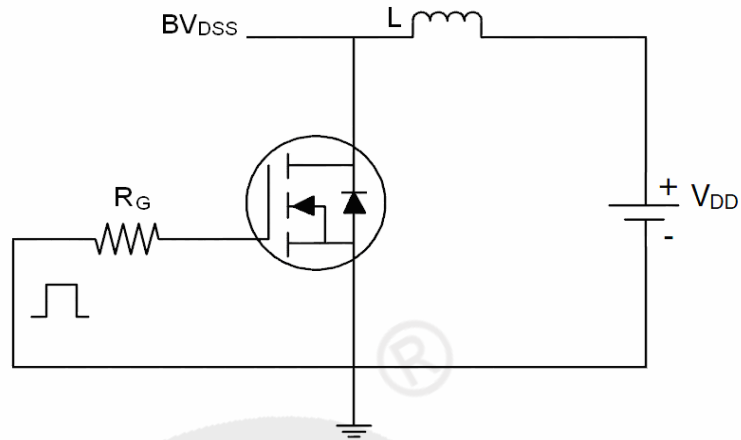
Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	75	86	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=75V, V_{GS}=0V$	-	-	1	μA	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 200	nA	
On Characteristics							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	25°C	-	3.5	4.5	m Ω
			125°C	-	5.7	7.4	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=40A$	100	165	-	S	
Dynamic Characteristics							
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	12100	-	PF	
Output Capacitance	C_{oss}		-	2000	-	PF	
Reverse Transfer Capacitance	C_{rss}		-	480	-	PF	
Switching Characteristics							
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=38V, I_D=40A$ $V_{GS}=10V, R_{GEN}=1.2\Omega$ (Note2)	-	20	-	nS	
Turn-on Rise Time	t_r		-	190	-	nS	
Turn-Off Delay Time	$t_{d(off)}$		-	130	-	nS	
Turn-Off Fall Time	t_f		-	120	-	nS	
Total Gate Charge	Q_g	$V_{DS}=60V, I_D=40A,$ $V_{GS}=10V$ (Note2)	-	410	620	nC	
Gate-Source Charge	Q_{gs}		-	90	140	nC	
Gate-Drain Charge	Q_{gd}		-	140	210	nC	
Drain-Source Diode Characteristics							
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V	
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = 40A$ $di/dt = 100A/\mu s$ (Note2)	-	120	210	nS	
Reverse Recovery Charge	Q_{rr}		-	860	1300	nC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)					

Notes:

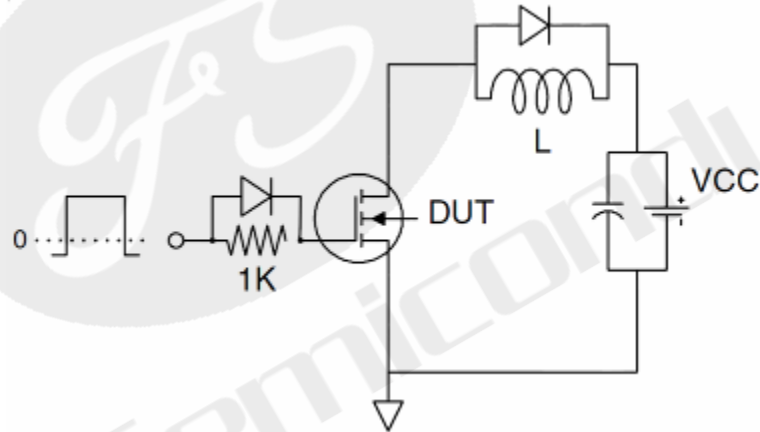
- Surface Mounted on FR4 Board, $t \leq 10$ sec.
- Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
- EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=37.5V, V_G=10V, L=2mH, R_g=25\Omega, I_{AS}=37A$
- $ISD \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V(BR)_{DSS}, T_J \leq 175^{\circ}\text{C}$
- Package limitation current is 190A.

Test circuit

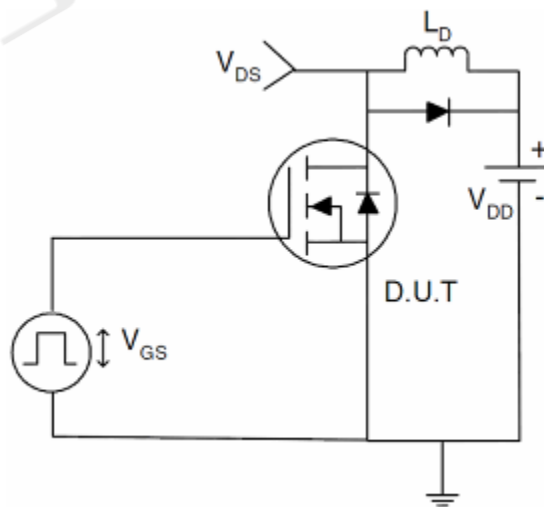
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:





Typical Electrical And Thermal Characteristics(Curves)

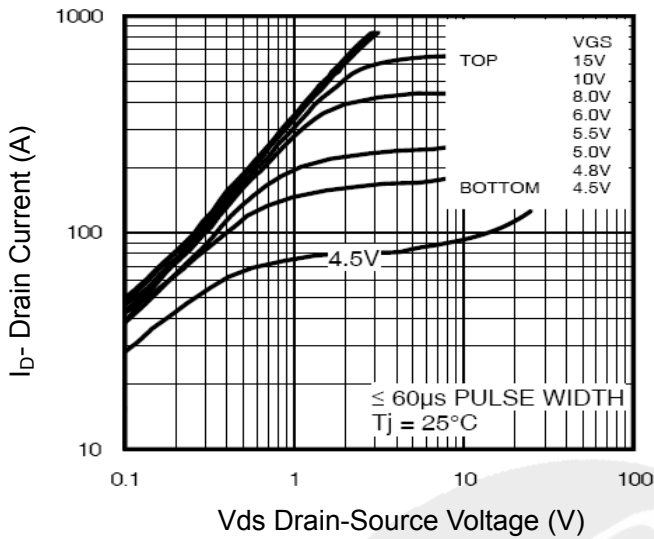


Figure 1 Output Characteristics

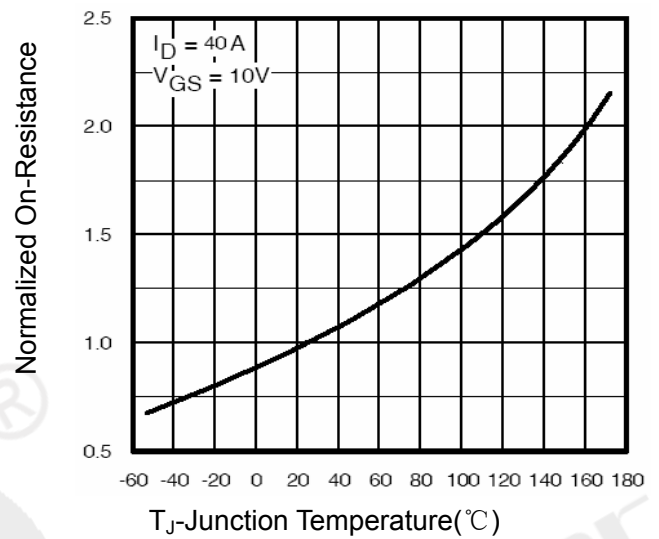


Figure 4 Rds(on)-Junction Temperature

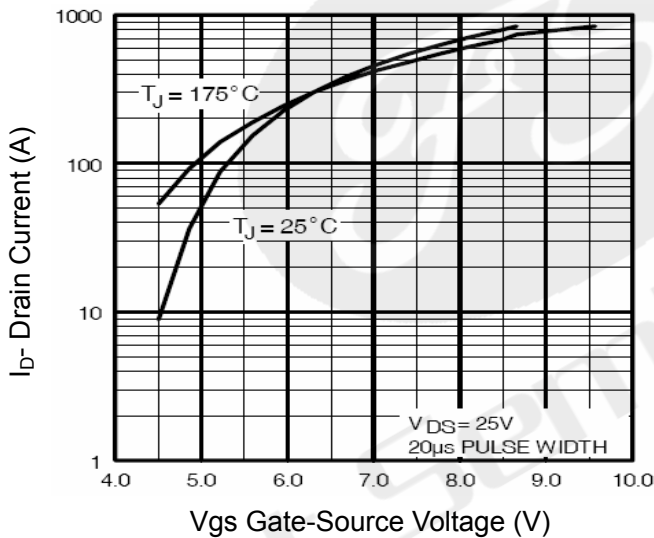


Figure 2 Transfer Characteristics

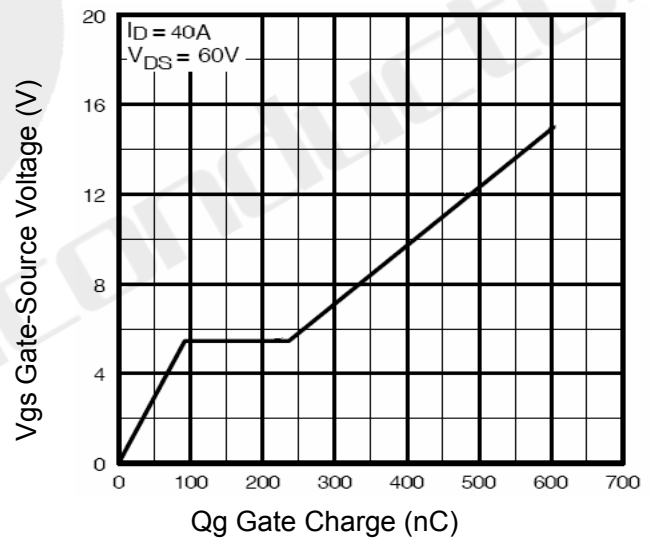


Figure 5 Gate Charge

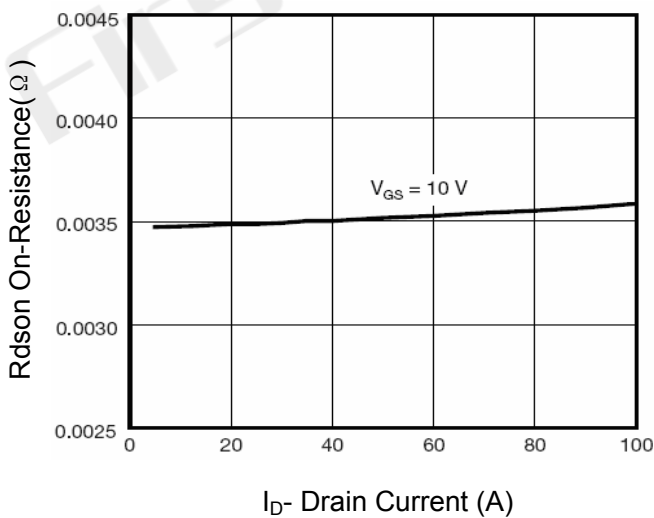


Figure 3 Rds(on)- Drain Current

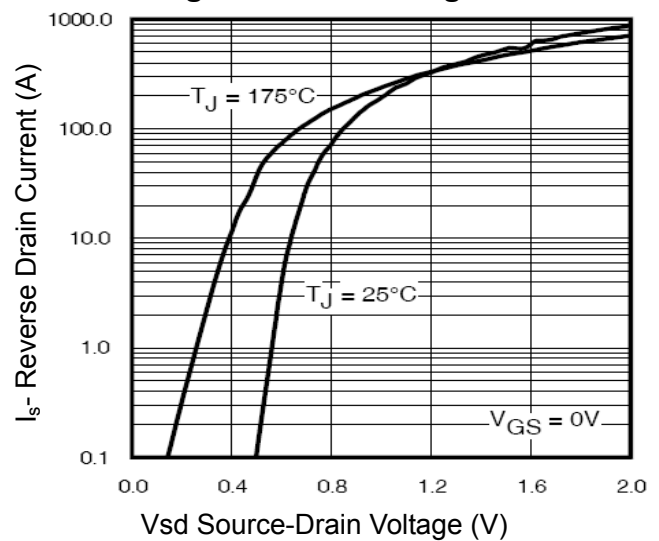


Figure 6 Source- Drain Diode Forward

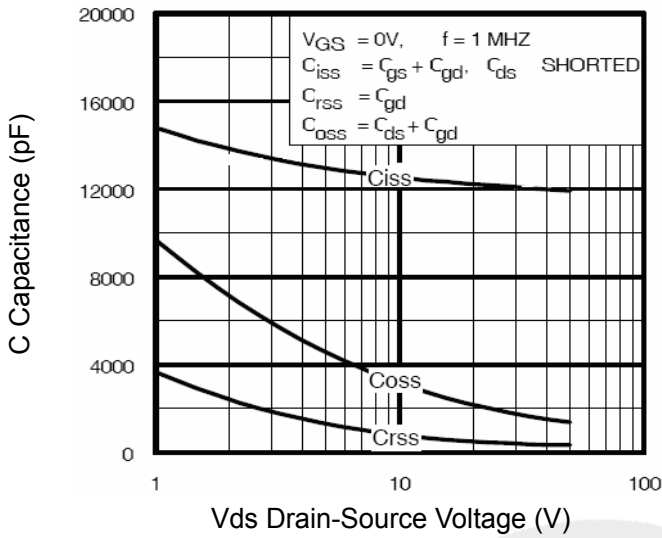


Figure 7 Capacitance vs Vds

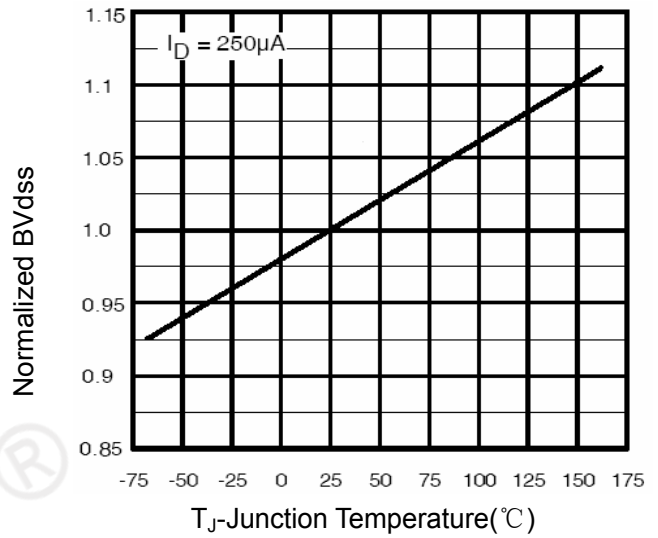


Figure 9 BV_{DSS} vs Junction Temperature

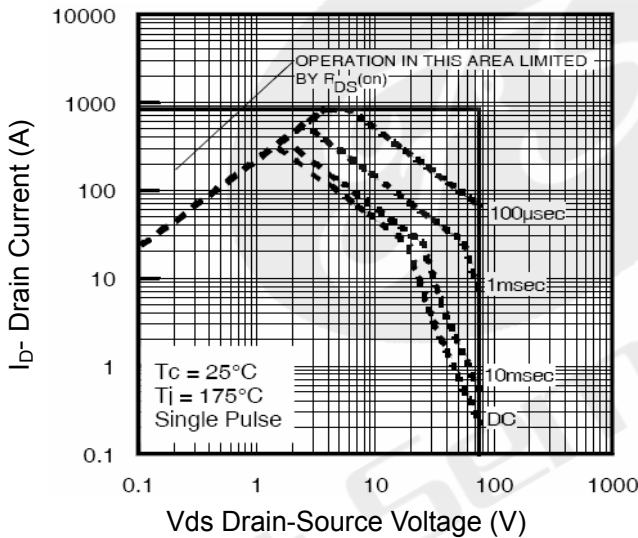


Figure 8 Safe Operation Area

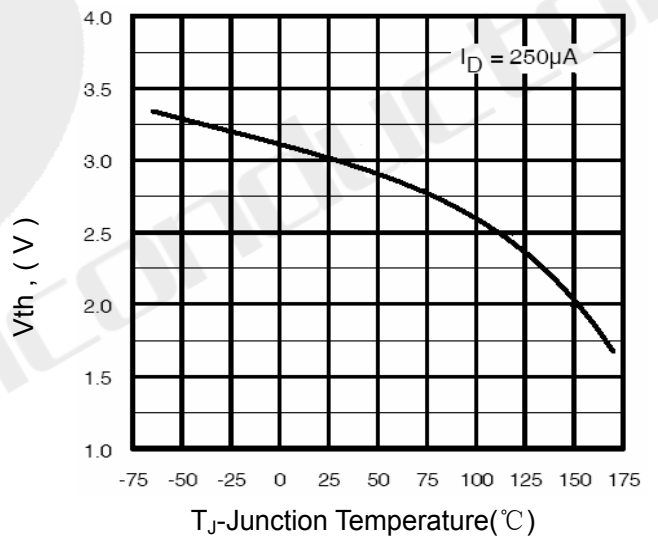


Figure 10 $V_{GS(th)}$ vs Junction Temperature

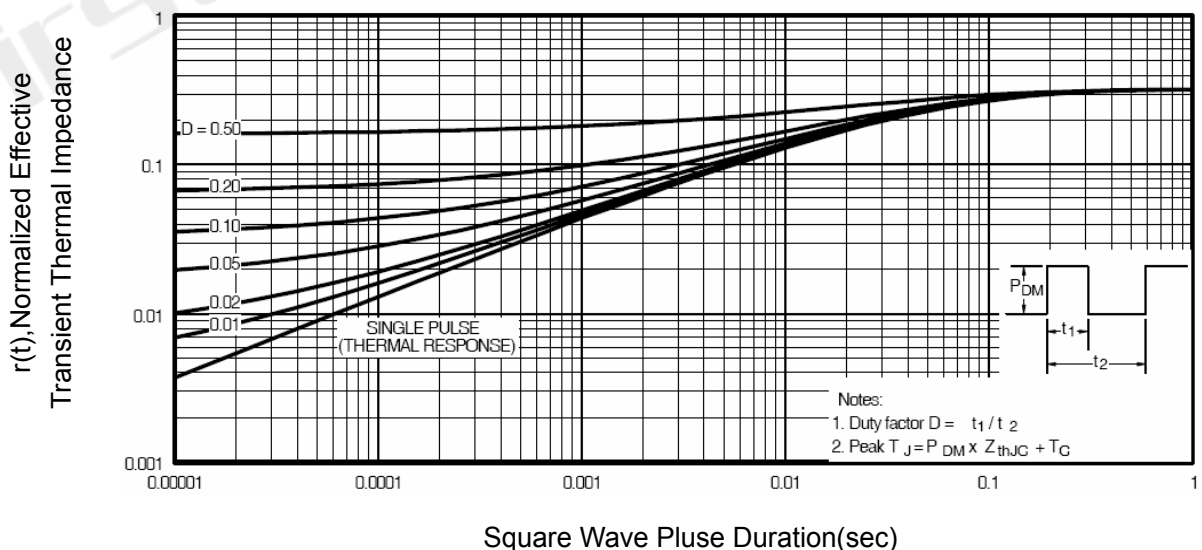
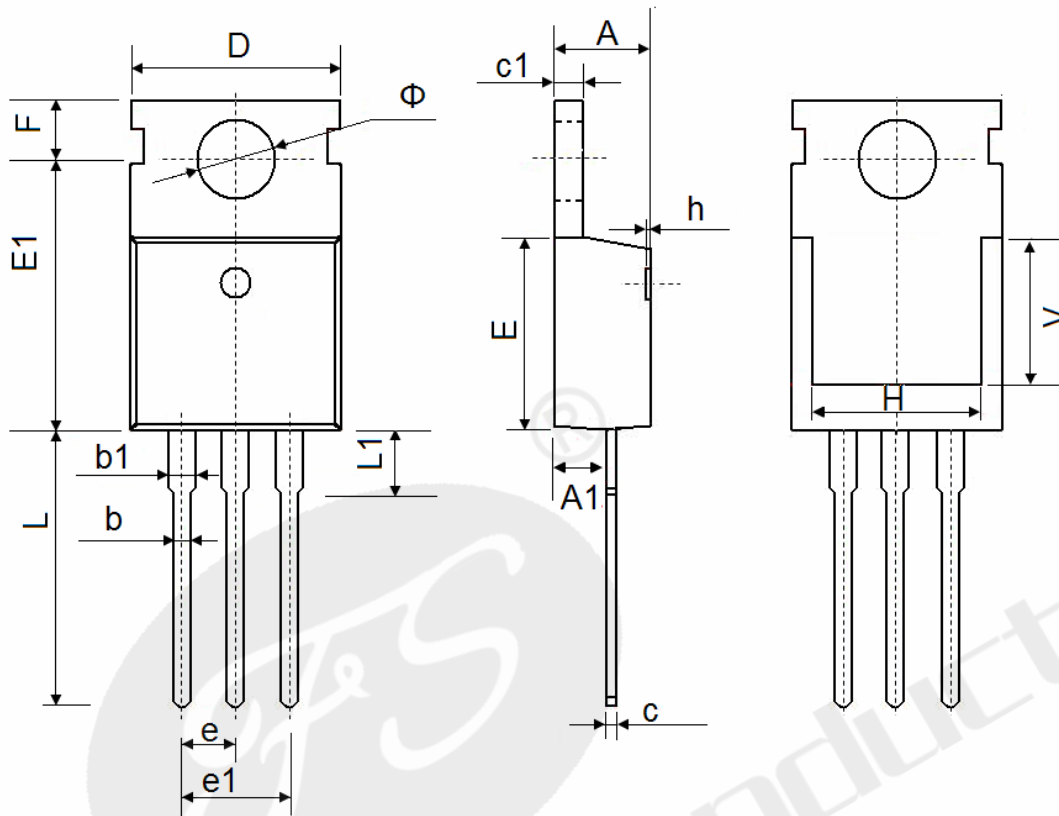


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-220AB Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	