First Semiconductor

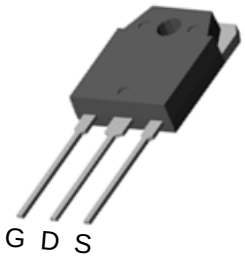
FIR210N075ANG

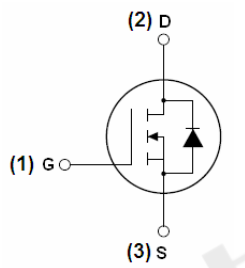
N-Channel Enhancement Mode Power Mosfet

Description

The FIR210N075TG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

PIN Connection TO-3P





General Features

- V_{DSS} =75V,I_D =210A
  $R_{DS(ON)}$ < 4mΩ @ V_{GS}=10V
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Automotive applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Marking Diagram

Y	= Year
A	= Assembly Location
WW	= Work Week
FIR210N075AN	= Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR210N075T	FIR210N075TG	TO-3P/TO-247	-	-	-

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	75	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	150	A
Pulsed Drain Current	I_{DM}	840	A
Maximum Power Dissipation	P_D	330	W
Derating factor		2.2	W/℃
Single pulse avalanche energy (Note 4)	E_{AS}	2200	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 1)	$R_{\theta JC}$	0.455	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V I_D=250μA	75			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=75V,V_{GS}=0V			1	μA
Gate-Body Leakage Current		I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±200	nA
On Characteristics							
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	25℃	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A		2.9	4	mΩ
	125℃				4.7	6.5	mΩ
Forward Transconductance		g_{FS}	V_{DS}=25V,I_D=40A	100	165		S
Dynamic Characteristics							
Input Capacitance		C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		11000		PF
Output Capacitance		C_{oss}			914		PF
Reverse Transfer Capacitance		C_{rss}			695		PF
Switching Characteristics							
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω		23		nS
Turn-on Rise Time		t_r			190		nS
Turn-Off Delay Time		$t_{d(off)}$			130		nS
Turn-Off Fall Time		t_f			120		nS
Total Gate Charge		Q_g	ID=30A,VDD=30V,VGS=10V	-	250	Q_g	nC
Gate-Source Charge		Q_{gs}		-	48	Q_{gs}	nC
Gate-Drain Charge		Q_{gd}		-	98	Q_{gd}	nC
Drain-Source Diode Characteristics							
Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=40A			1.2	V
Reverse Recovery Time		t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs(Note2)		48		nS
Reverse Recovery Charge		Qrr			78		nC
Forward Turn-On Time		t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

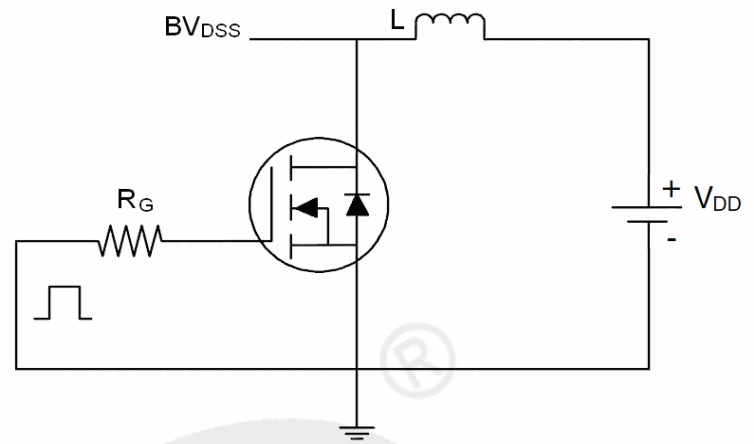
1. Surface Mounted on FR4 Board, t ≤ 10 sec.

2. Pulse Test: Pulse Width ≤ 400μs, Duty Cycle ≤ 2%.

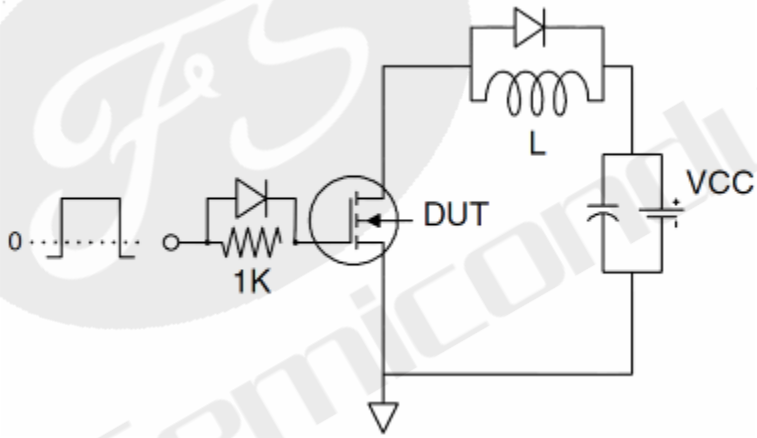
3. EAS condition：Tj=25℃,V_{DD}=37.5V,V_G=10V,L=2mH,Rg=25Ω,I_{AS}=37A

Test circuit

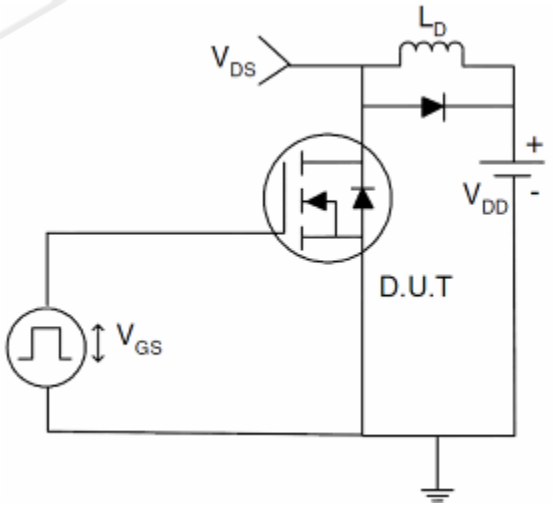
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit：



Typical Electrical And Thermal Characteristics(Curves)

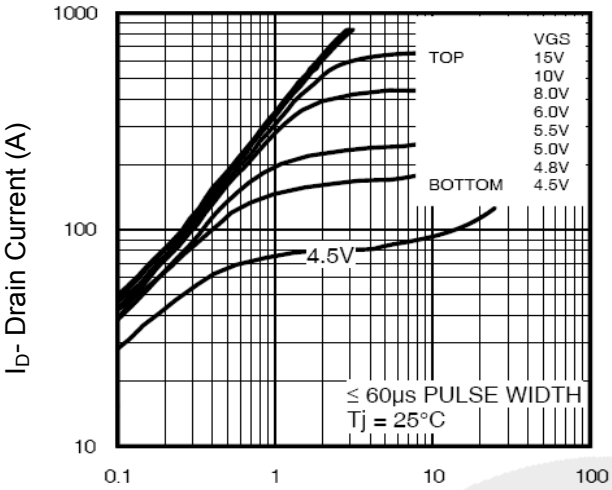


Figure 1 Output Characteristics

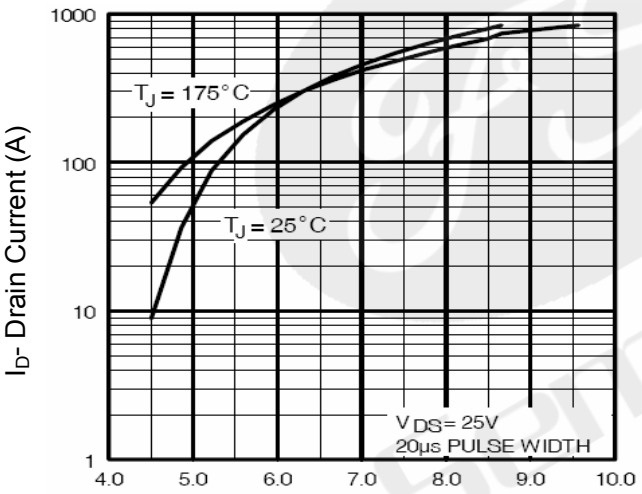


Figure 2 Transfer Characteristics

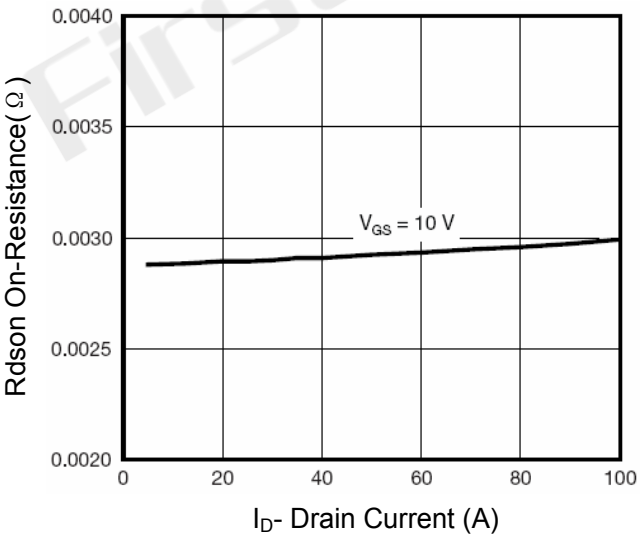


Figure 3 Rdson- Drain Current

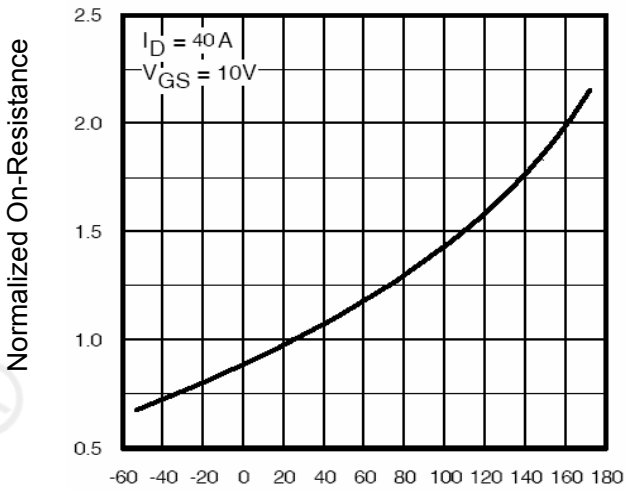


Figure 4 Rdson-JunctionTemperature

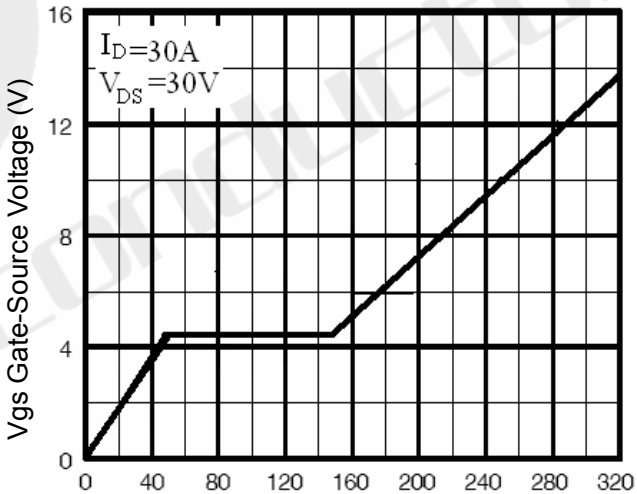


Figure 5 Gate Charge

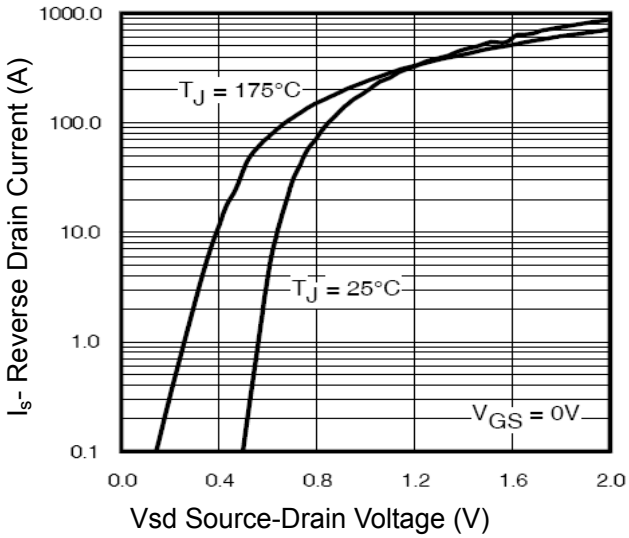


Figure 6 Source- Drain Diode Forward

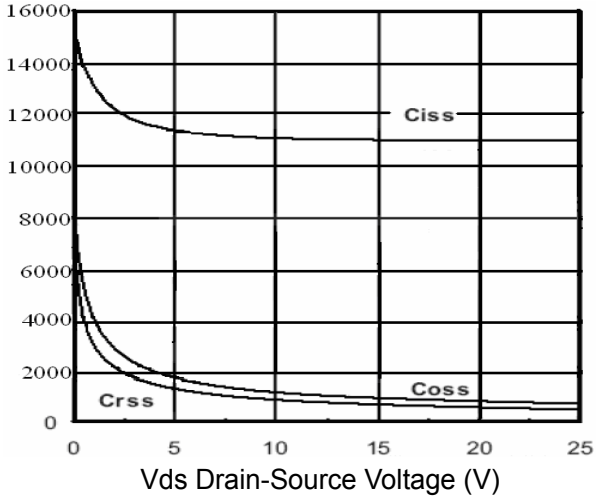


Figure 7 Capacitance vs Vds

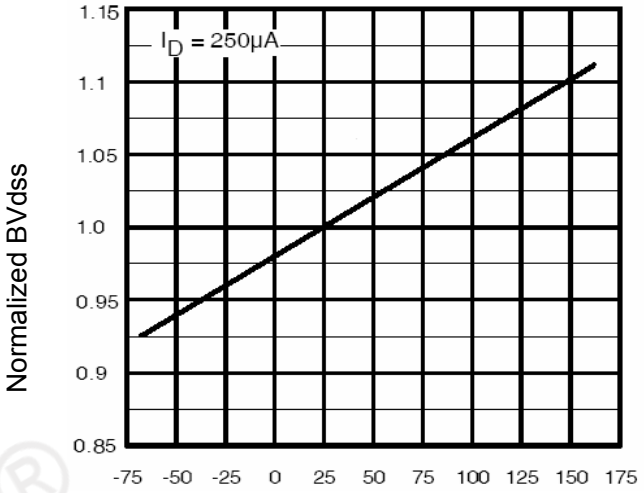


Figure 9 BV_{DSS} vs Junction Temperature

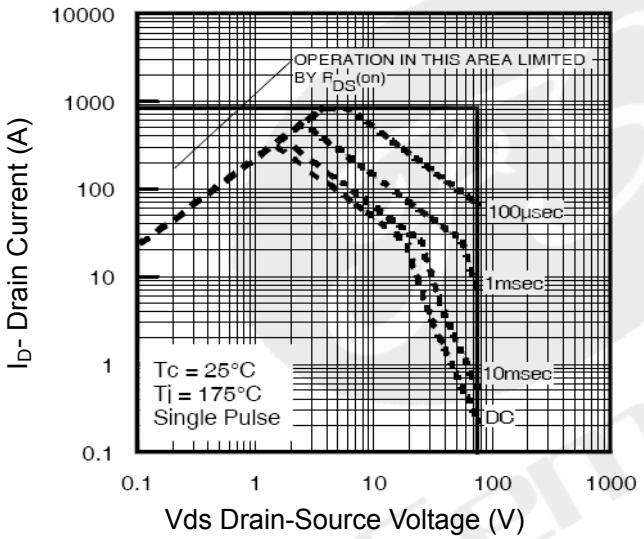


Figure 8 Safe Operation Area

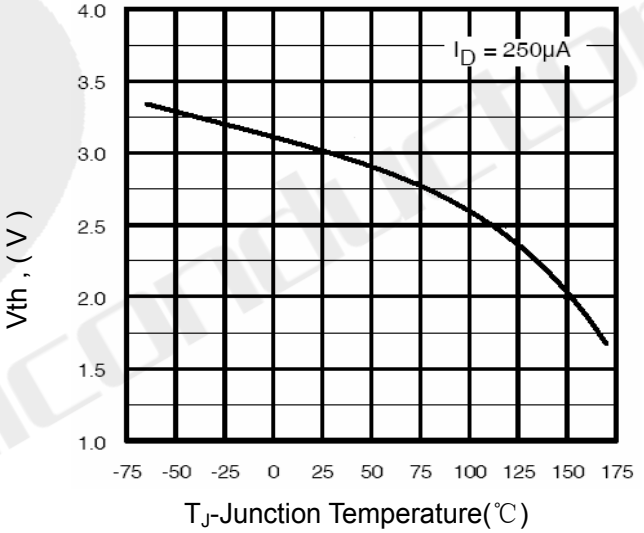


Figure 10 $V_{GS(th)}$ vs Junction Temperatur

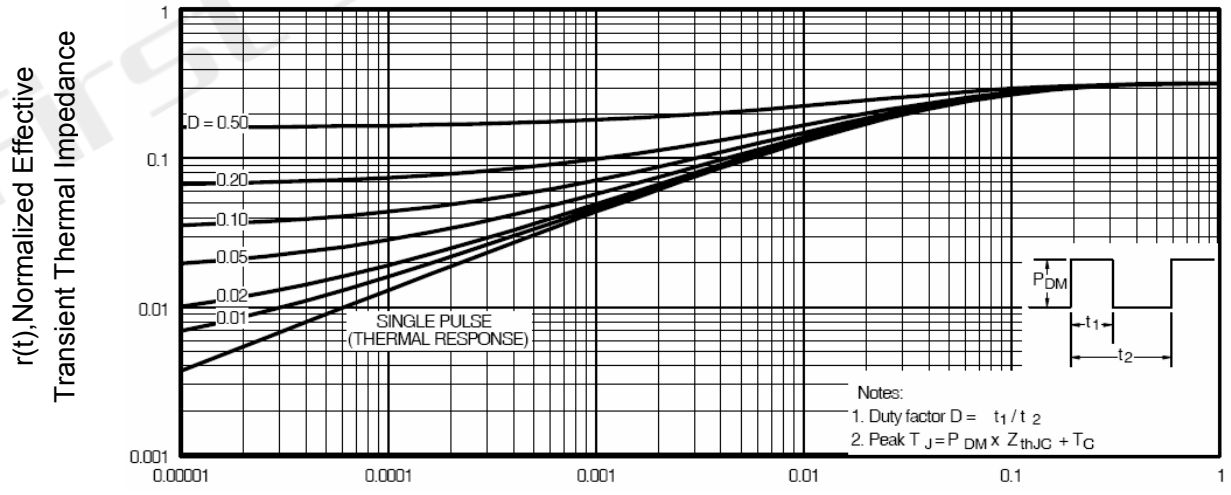
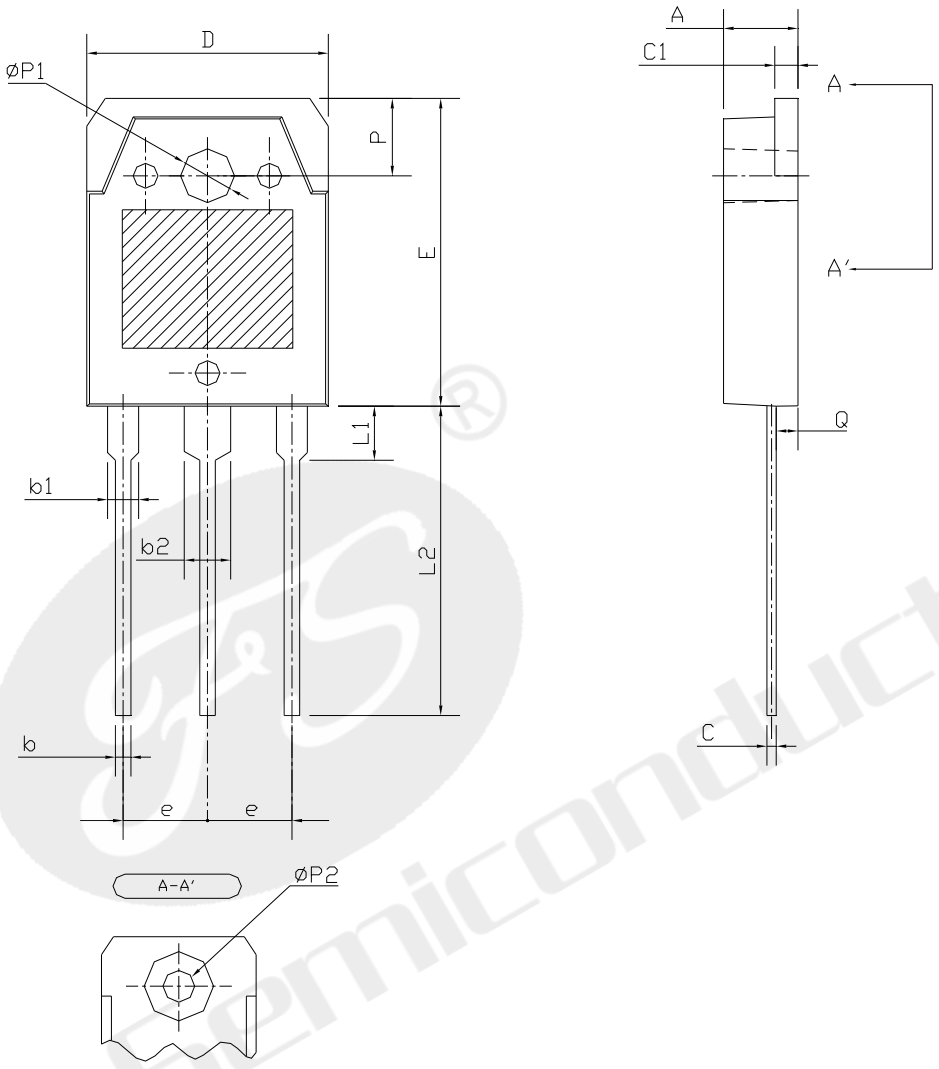


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Outline Dimensions



SYMBOL	MIN	NOM	MAX
A	4.60	4.80	5.00
b	0.80	1.00	1.20
b1	1.80	2.00	2.20
b2	2.80	3.00	3.20
C	0.55	0.60	0.75
C1	1.45	1.50	1.65
D	15.40	15.60	15.80
E	19.70	19.90	20.10
e	5.15	5.45	5.75
L1	3.30	3.50	3.70
L2	19.80	20.00	20.20
P	4.80	5.00	5.20
ØP1	3.30	3.40	3.50
ØP2		(3.20)	
Q	1.20	1.40	1.60

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	