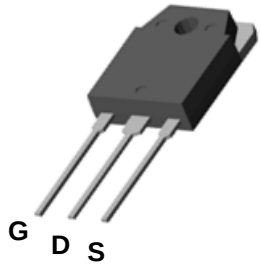
N-Channel Power MOSFET

PIN Connection TO-3P

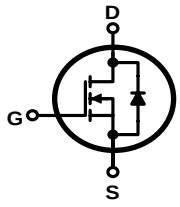


Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
FIR28N60ANG	650 V	0.150 Ω	28 A

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Schematic diagram



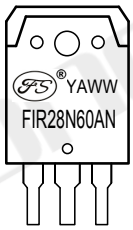
Applications

- Switching applications
- LCC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Qg. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Marking Diagram



Y	= Year
A	= Assembly Location
WW	= Work Week
FIR28N60AN	= Specific Device Code

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	28(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	14(1)	A
I_{DM} (2)	Drain current (pulsed)	88(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature		

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 28$ A, di/dt ≤ 400 A/μs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}= 400 V.
4. $V_{DS} \leq 480$ V

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.17	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50)	2200	mJ

Electrical characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V			1	μA
		V_{DS} = 600 V, T_C=125 °C			100	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±10	μA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14 A		0.135	0.150	Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1440	-	pF
C_{oss}	Output capacitance		-	70	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	104	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 28 A, V_{GS} = 10 V (see *Figure 15*)	-	36	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 14 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14* and *Figure 19*)	-	14.5	-	ns
t_r	Rise time		-	7.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	100	-	ns
t_f	Fall time		-	8	-	ns

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
I_{SDM} (1)	Source-drain current (pulsed)		-		88	A
V_{SD} (2)	Forward on voltage	I_{SD} = 28 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 28 A, di/dt = 100 A/μs V_{DD} = 60 V (see *Figure 19*)	-	350		ns
Q_{rr}	Reverse recovery charge		-	4.7		μC
I_{RRM}	Reverse recovery current		-	27		A
t_{rr}	Reverse recovery time	I_{SD} = 28 A, di/dt = 100 A/μs V_{DD} = 60 V, T_j = 150 °C (see *Figure 19*)	-	451		ns
Q_{rr}	Reverse recovery charge		-	6.5		μC
I_{RRM}	Reverse recovery current		-	29		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

Electrical characteristics (curves)

Figure 2. Safe operating area

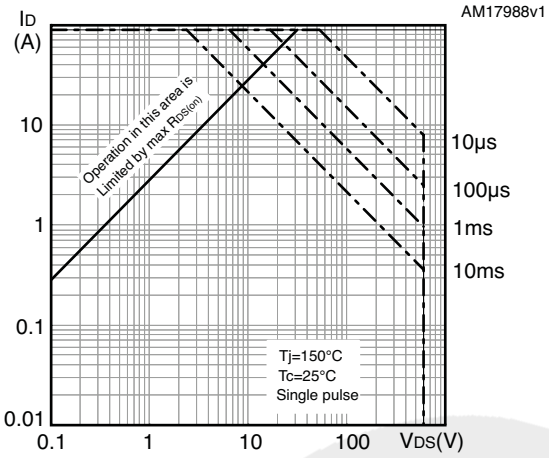


Figure 3. Thermal impedance

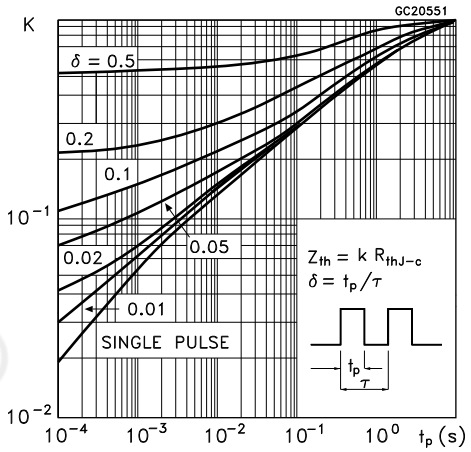


Figure 4. Output characteristics

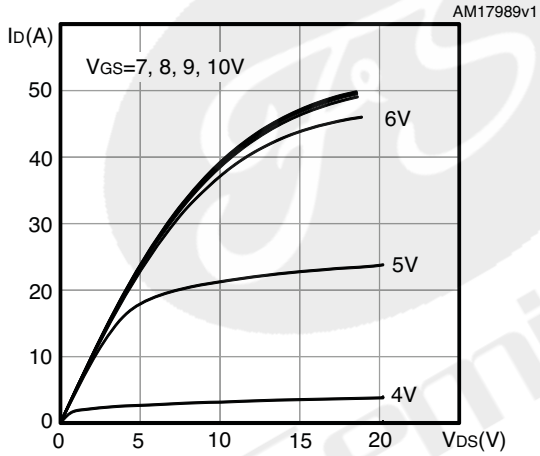


Figure 5. Transfer characteristics

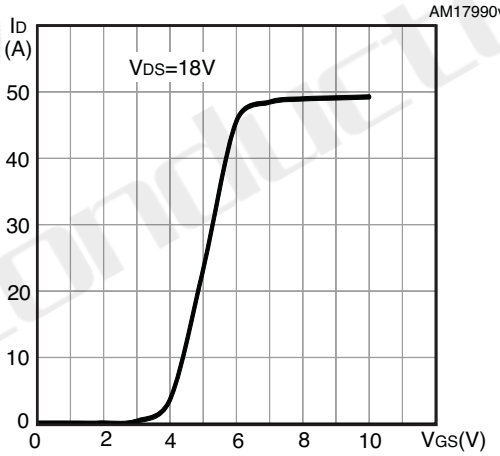


Figure 6. Gate charge vs gate-source voltage

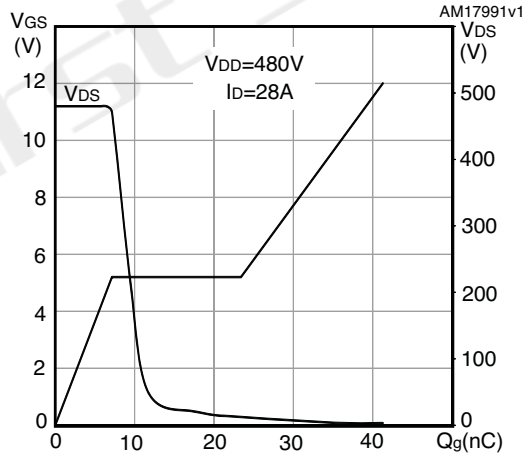


Figure 7. Static drain-source on-resistance

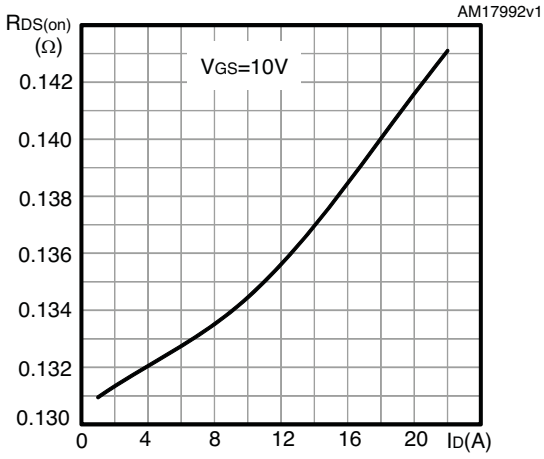


Figure 8. Capacitance variations

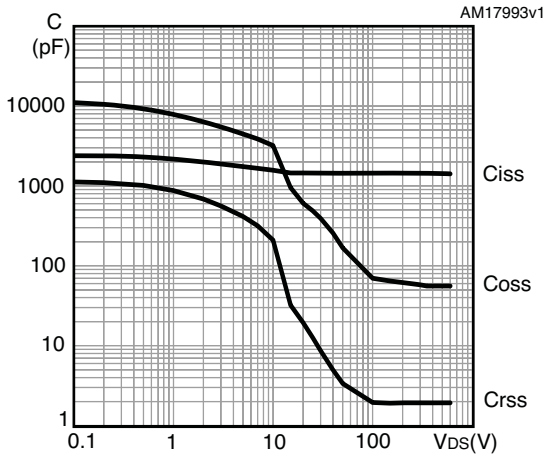


Figure 9. Output capacitance stored energy

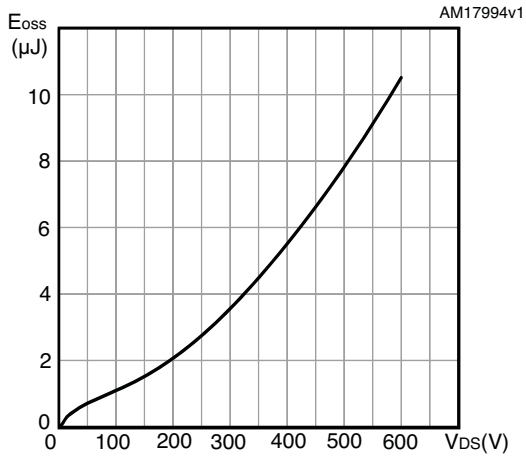


Figure 10. Normalized gate threshold voltage vs temperature

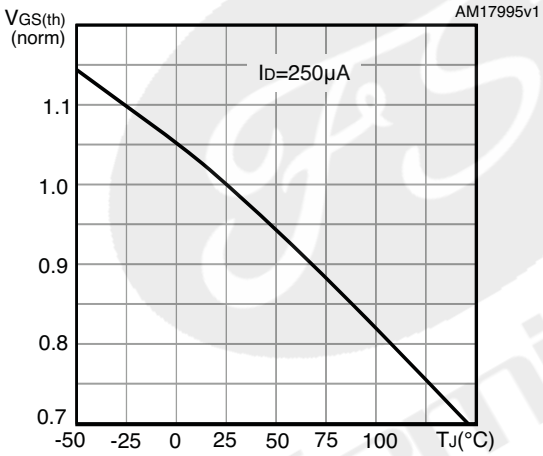


Figure 11. Normalized on-resistance vs temperature

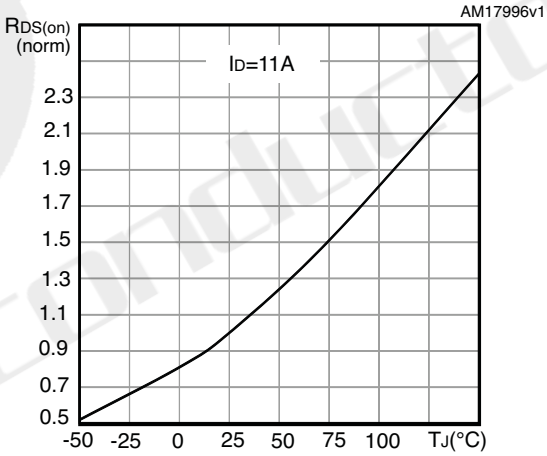


Figure 12. Normalized V_{DS} vs temperature

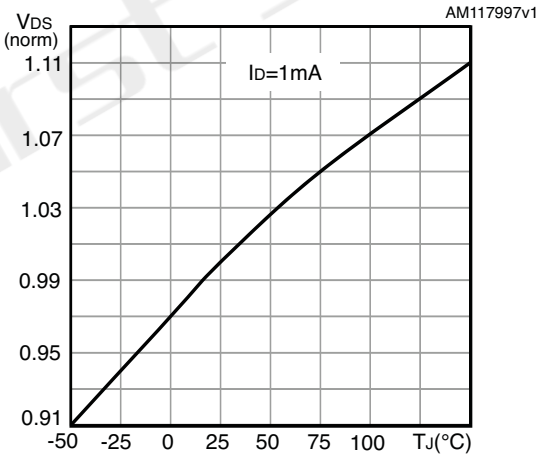
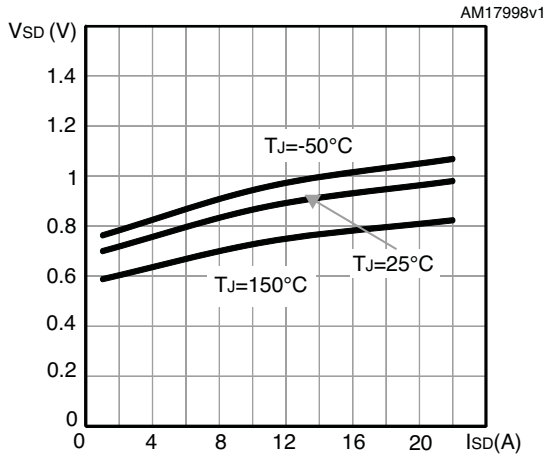


Figure 13. Source-drain diode forward characteristics



Test circuits

Figure 14. Switching times test circuit for resistive load

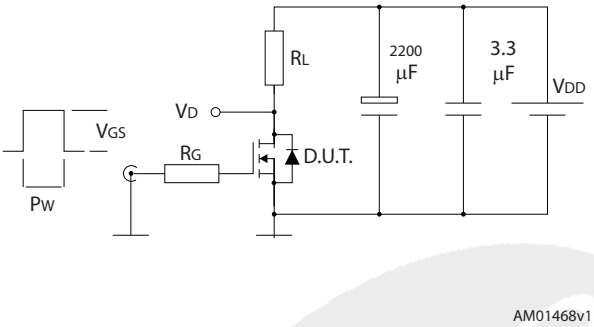


Figure 15. Gate charge test circuit

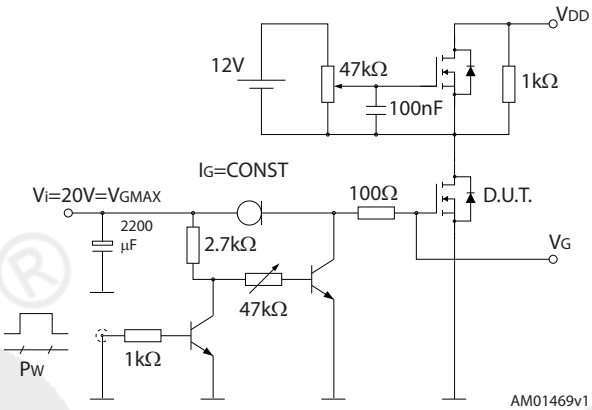


Figure 16. Test circuit for inductive load switching and diode recovery times

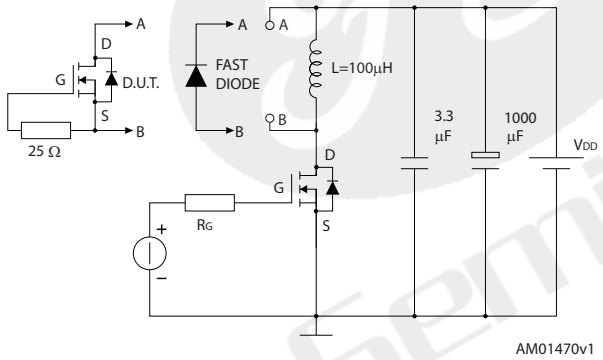


Figure 17. Unclamped inductive load test circuit

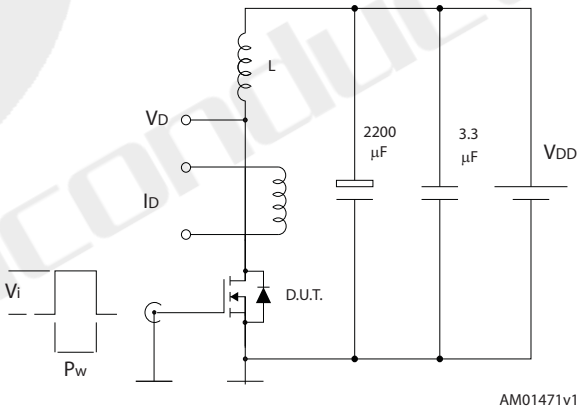


Figure 18. Unclamped inductive waveform

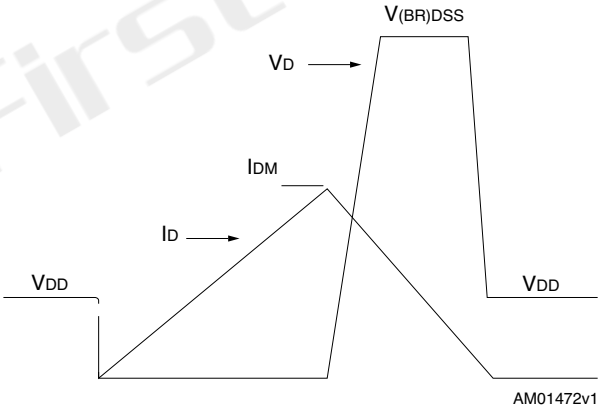
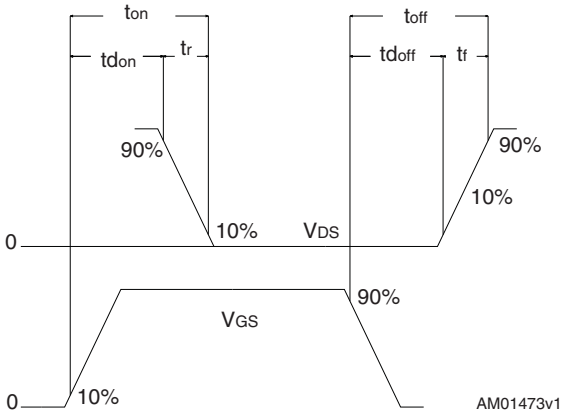


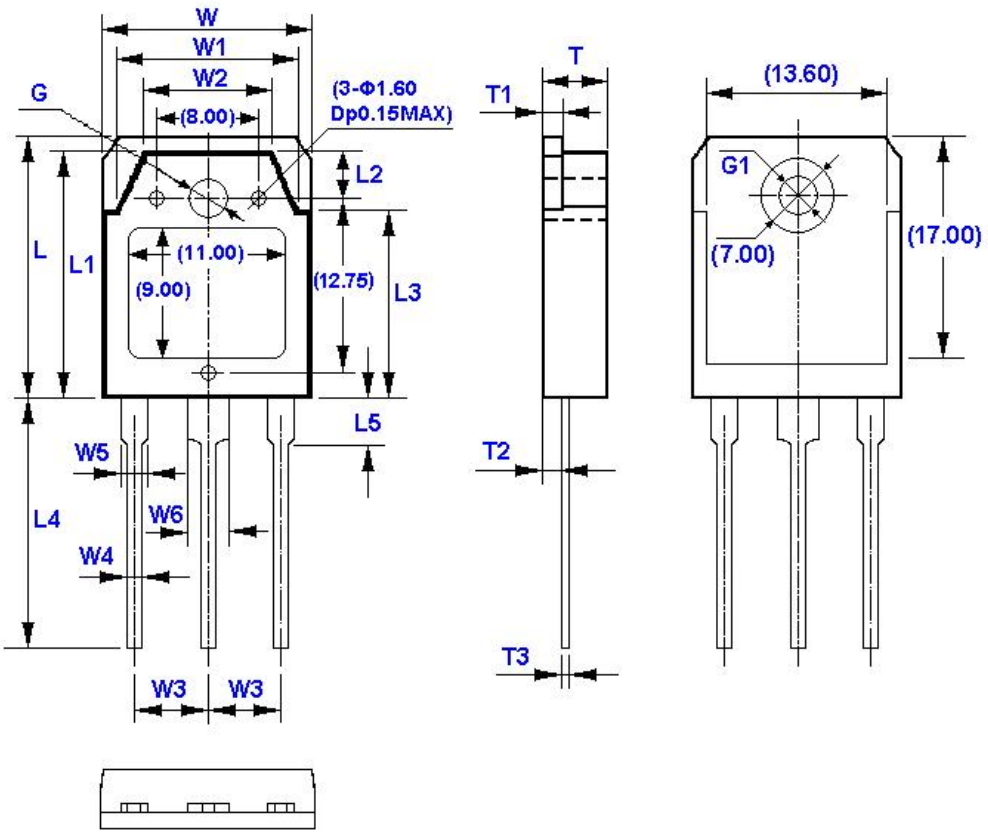
Figure 19. Switching time waveform



Package Outline Dimensions

TO-3P

Units：mm



符号	尺寸		符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max		Min	Max
W	15.40	15.80	W5	1.80	2.20	L3	13.70	14.10	T2	1.20	1.60
W1	13.40	13.80	W6	2.80	3.20	L4	19.70	20.30	T3	0.55	0.75
W2	9.40	9.80	L	19.70	20.10	L5	3.30	3.70	G (Φ) (正面)	3.30	3.50
W3	5.45 (TYP)		L1	18.50	18.90	T	4.60	5.00	G1(Φ) (背面)	3.10	3.30
W4	0.80	1.20	L2	3.60	4.00	T1	1.45	1.65			

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	