## General Description

FIR4N65LG , the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252 , which accords with the RoHS standard.
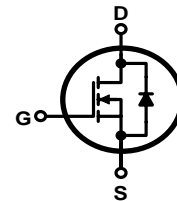
Features

- l **Fast Switching**
- l **ESD Improved Capability**
- l **Low Gate Charge**
- l **Low Reverse transfer capacitances**
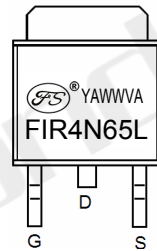- l **100% Single Pulse avalanche energy Test**

PIN Connection TO-252(D-PAK)
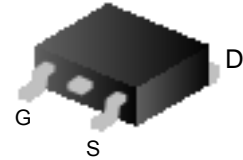
Schematic diagram

Marking Diagram

YAWWVA
FIR4N65L

Y	= Year
A	= Assembly Location
WW	= Work Week
VA	= Version &Assembly plant
FIR4N65L	= Specific Device Code

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted; reference only)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	4.0	A
	T_C=100°C		2.5	
Drain Current Pulsed		I_{DM}	16	A
Power Dissipation(T_C=25°C)		P_D	75	W
-Derate above 25°C			0.6	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	200	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

Thermal Characteristics

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	110	°C/W

Electrical Characteristics (Ta = 25°C unless otherwise noted; reference only)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	25 °C, V_{GS}=0V, I_D=250µA	650	--	--	V
		125°C, V_{GS}=0V, I_D=250µA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	25 °C, V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		125°C, V_{DS}=520V, V_{GS}=0V	--	--	100	uA
		150°C, V_{DS}=520V, V_{GS}=0V	--	--	100	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250µA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2A	--	2.4	2.8	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ		610		pF
Output Capacitance	C_{oss}		--	53	--	
Reverse Transfer Capacitance	C_{rss}		--	3.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V,I_D=4.0A, R_G=10Ω	--	14	--	ns
Turn-on Rise Time	t_r		--	16	--	
Turn-off Delay Time	$t_{d(off)}$		--	32	--	
Turn-off Fall Time	t_f	(Note 2,3)	--	11	--	
Total Gate Charge	Q_g	V_{DS}=520V,I_D=4.0A, V_{GS}=10V	--	14.5	--	nC
Gate-Source Charge	Q_{gs}		--	3	--	
Gate-Drain Charge	Q_{gd}	(Note 2,3)	--	6.5	--	

Source-Drain Diode Ratings And Characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/µs	--	256	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.2	--	µC

Notes:

1. L=10mH,I_{AS}= 6.3 A,V_{DD}=100V, R_G=10Ω, starting T_J=25°C;

2. Pulse Test: Pulse width ≤300µs,Duty cycle≤2%;

3. Essentially independent of operating temperature.
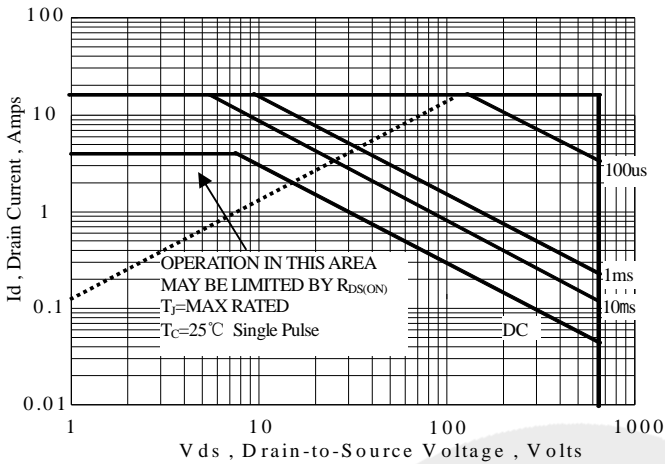
Characteristics Curve

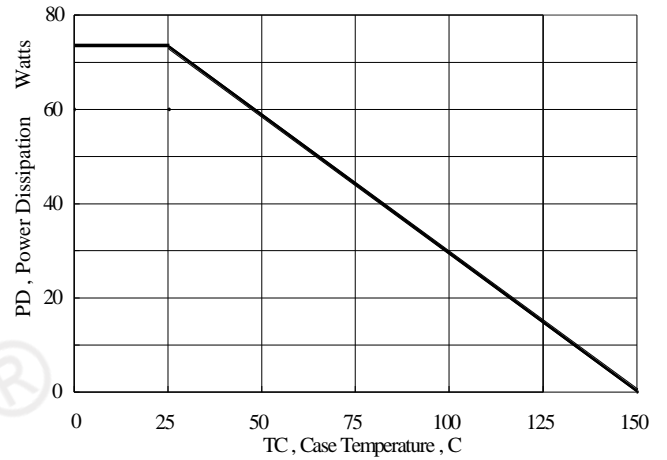Figure 1 Maximum Forward Bias Safe Operating Area
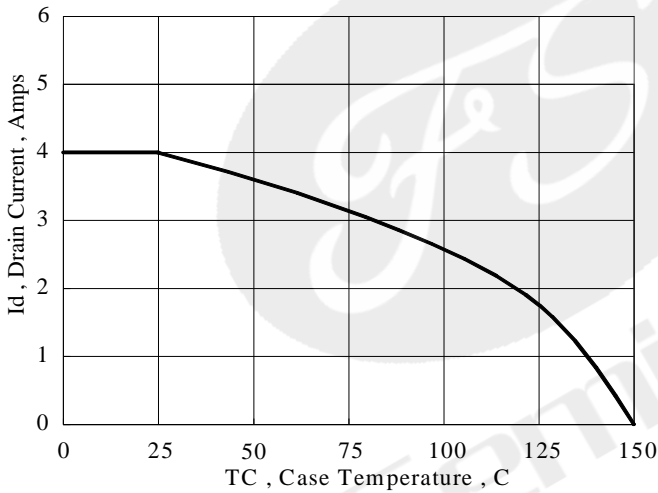

Figure 2 Maximum Power Dissipation vs Case Temperature

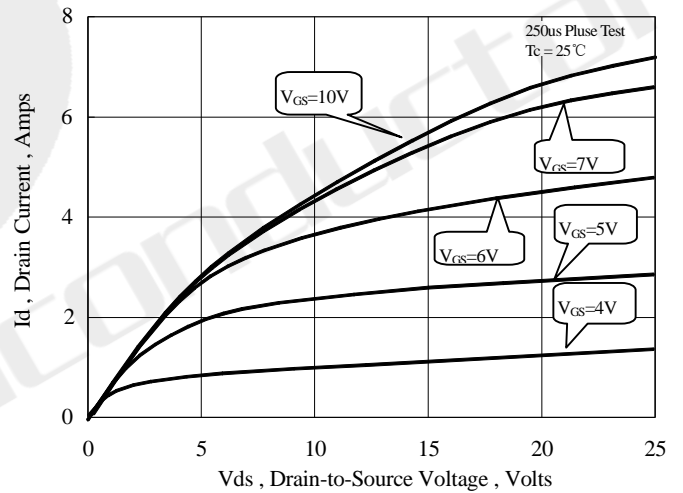Figure 3 Maximum Continuous Drain Current vs Case Temperature
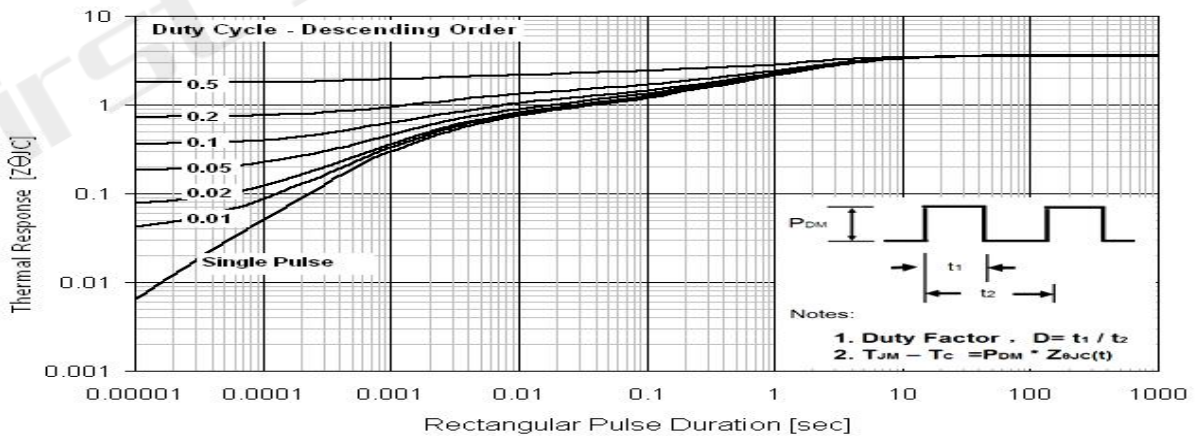

Figure 4 Typical Output Characteristics

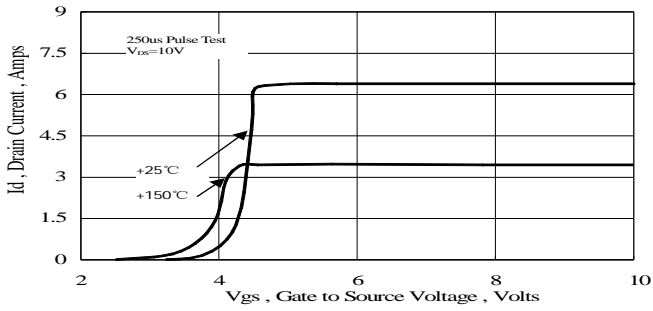Fi e 5 Maximum Effective Thermal Im endance unction to Case

![First Semiconductor logo]

Figure 6 Typical Transfer Characteristics
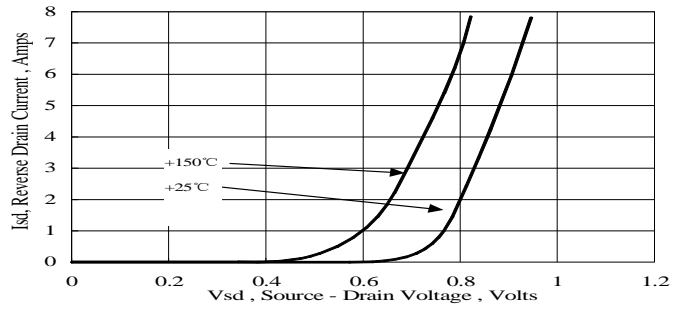
Figure 7 Typical Body Diode Transfer Characteristics
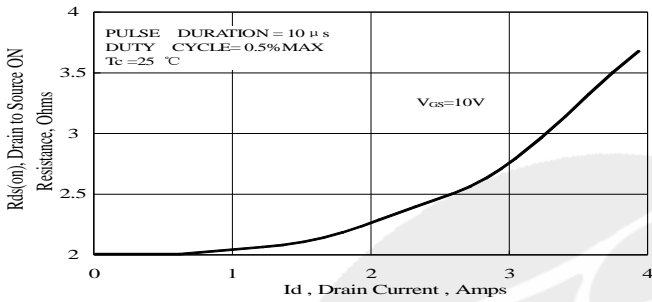
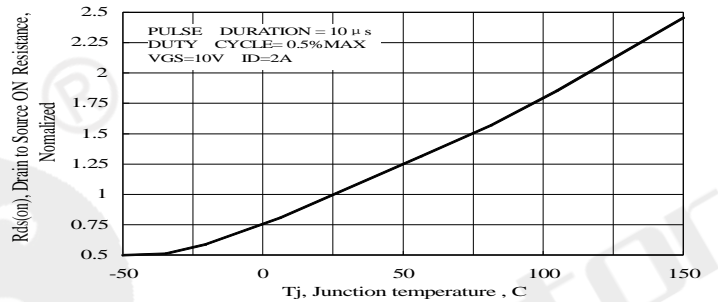Figure 8 Typical Drain to Source ON Resistance vs Drain Current

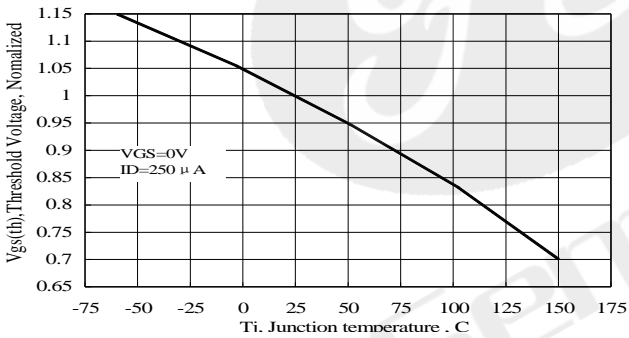Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

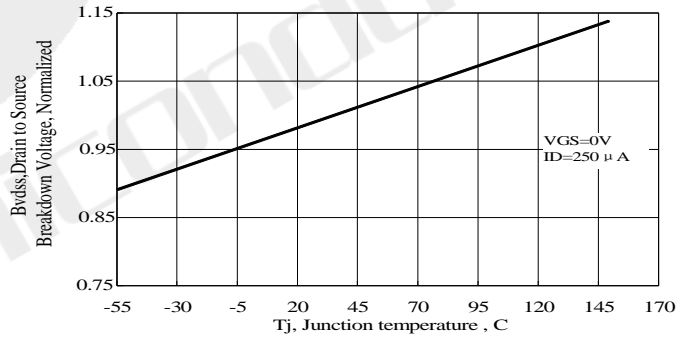Figure 10 Typical Theshold Voltage vs Junction Temperature

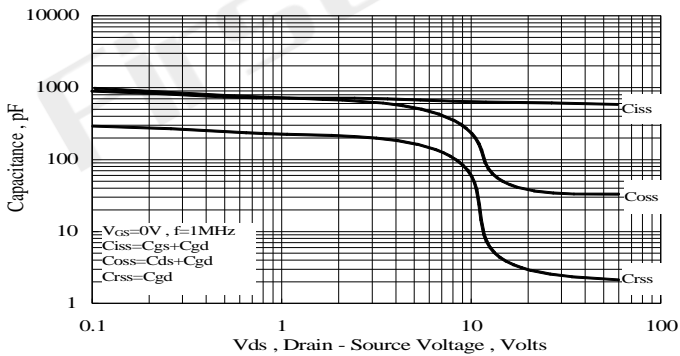Figure 11 Typical Breakdown Voltage vs Junction Temperature
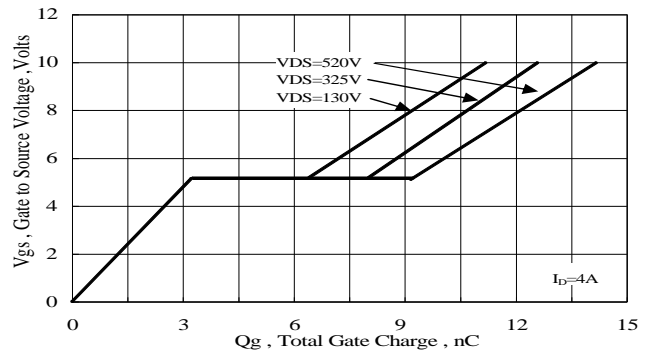
Figure 12 Typical Capacitance vs Drain to Source Voltage

Figure 13 Typical Gate Charge vs Gate to Source Voltage
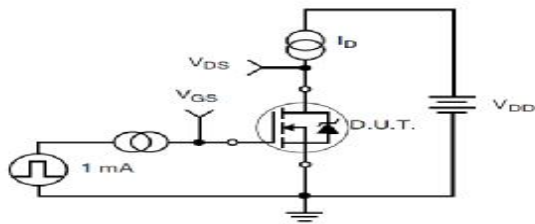
Typical Test Circuit
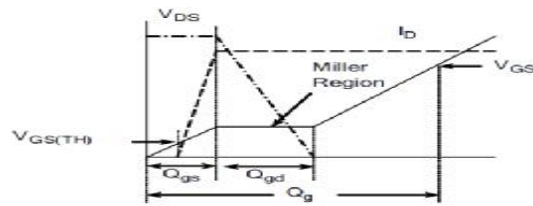
Figure 17. Gate Charge Test Circuit
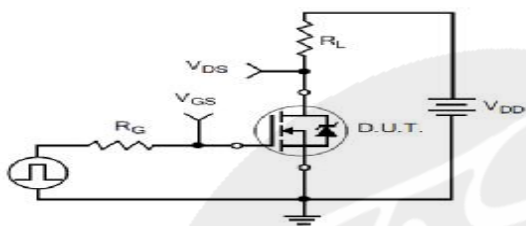
Figure 18. Gate Charge Waveform

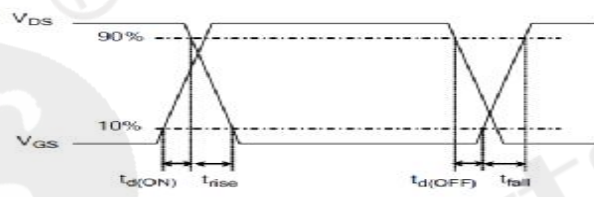Figure 19. Resistive Switching Test Circuit
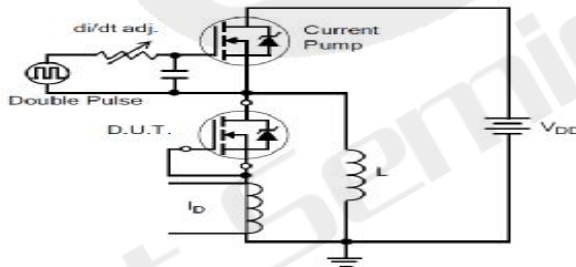
Figure 20. Resistive Switching Waveforms

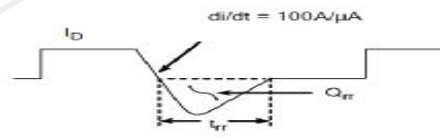Figure 21. Diode Reverse Recovery Test Circuit

Figure 22. Diode Reverse Recovery Waveform

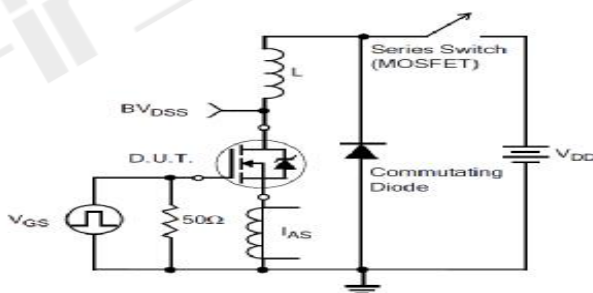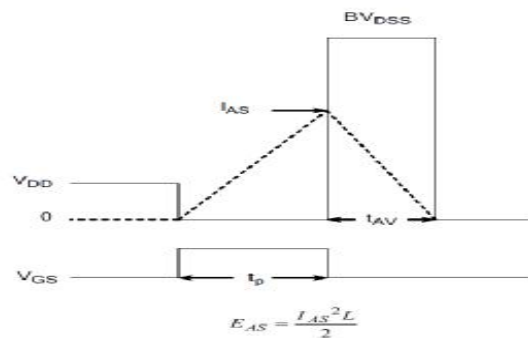Figure 23. Unclamped Inductive Switching Test Circuit

Figure 24. Unclamped Inductive Switching Waveforms

$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Package Dimensions

TO-252

Units: mm
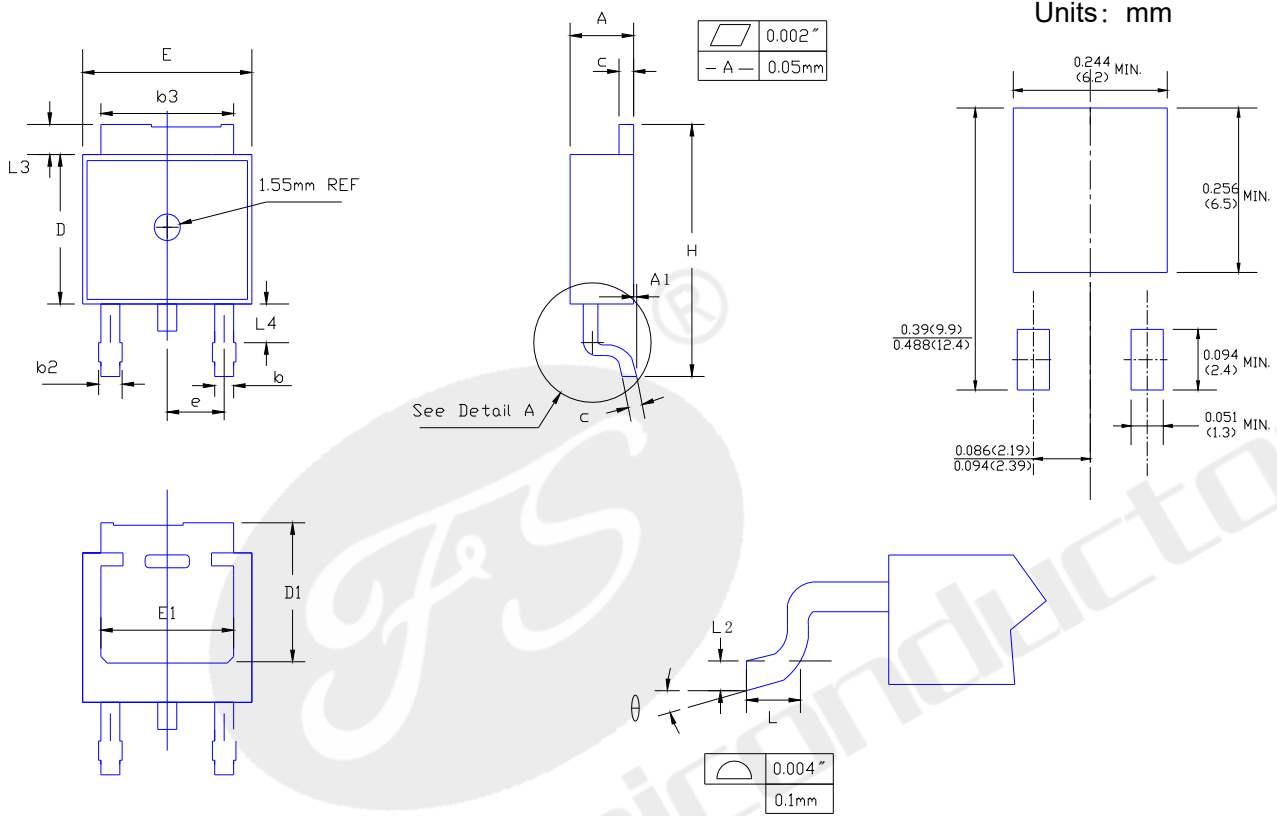
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	
A1	-	0.005	-	0.13	
b	0.025	0.035	0.64	0.89	
b2	0.033	0.045	0.84	1.14	
b3	0.205	0.215	5.21	5.46	
c	0.018	0.024	0.46	0.61	
D	0.241	0.249	6.12	6.32	
D1	0.205	-	5.21	-	
E	0.250	0.265	6.35	6.73	
E1	0.190	-	4.83	-	
e	0.090 BSC.		2.29 BSC.		
H	0.380	0.410	9.65	10.41	
L	0.055	0.070	1.40	1.78	
L2	0.020 BSC.		0.51 BSC.		
L3	0.035	0.050	0.89	1.27	
L4	0.025	0.040	0.64	1.01	
	0°	8°	0°	8°	

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.

- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety
  standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!

- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	